

CHASSIS SERVICE MANUAL

Chassis: 8M 59B

File Name: _____

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Draft by: _____

Checked by: _____

Approved by: _____

Release Date: 2010

Warning

The manual is only for the personnel who has the experience in TV repairing. There is no warning alarm in this manual for the potential danger faced by the unprofessional personnel who want to repair the TV set. To avoid the electric shock, refer the servicing to the qualified personnel.

1 General

1.1 Chassis Description

We named the chassis as 8M59B. The chassis can support the ISDB-T and PAL M, PAL N and NTSC M. The aim market is Brazil, Argentina and other South America country using ISDB-T terrestrial digital TV broadcasting.

1.2 Major Feature

ISDB-T Receive Full SEG;

PAL M, PAL N, NTSC M receive; 3

-HDMI input, 2-UPlayer, 2 Component input, 1 Composite input, 1 PC input, 1 composite output, 1 earphone output, 1 S/PDIF(Optical) output.

1.2 SPECIFICATION

Model #	32L05-8M59B	42L05-8M59B	47L05-8M59B
Country(West Eu./East Eu./Russia/AP/US/S.A./Japan/...)	Argentina		
Brand	Customer Brand		
Category (Monitor/TV/Combo/Portable TV...)	TV		
Panel technology (LCD / PDP)	LCD		
Market Position (High/Mid/Access,,)	Class		
Cabinet Design (Example: 01,23 series)	32L05	42L05	47L05
Product Nb	-		
Chassis solution	MST209+ISDB-T Demodulate		
Chassis name	8M59B		
Chassis PCB Standard	Skyworth RGB New Standard		
Predecessor (replace)	-		
MP date requested (ETD)	2010.7		
MP date confirmed by supplier (ETD/ETA)	-		
Status(Pre./Finish)	-		
Regional requirement			
Homologation (Gostandard/CE/MPTT/CB/...)	CB		
RoHS	Yes		
Power supply(100-240V AC +/-10%/...)	100-240V AC (-20%,+10%)		
Power consumption working / Annual	-		
Power consumption standby	<1W		
Power plug(VDE/UL/BS/...)	IRAM Plug		
Picture display			
Screen size : diagonale (inch)	32"	42"	47"
Aspect ratio (16/9 // 4/3 // 15/9)	16:9		
1st panel supplier : panel suppliers	LG		
1st panel supplier : panel reference			
Panel Display Type(MVA/PVA/IPS/...)	TFT LCD		
1st panel supplier : resolution	1366x768	1920x1080	1920x1080
Dynamic contrast ratio	50000 : 1	50000 : 1	50000 : 1
Video signal process			
Comb Filter (2D/3D)	3D		
Noise Reduction (adaptive/3D/...)	3D		
Picture improvement (LTI/CTI,BLE,WLE,...)	LTI / CTI		
Color process (Gama correction/Skin correction /...)	Dynamic brilliant and fresh color, Dynamic blue stretch, Dynamic vivid skin Programmable RGB gamma CLUT		
Colour preset (Cool/Normal/Warm/Personal)	Neutral, Cool, Warm and Personal		
Picture control (Bright/Con./Sharpness/Color/Tint/...)	Yes		
Picture presets : Standard / Bright / Soft / User	Personal/Soft/Bright/Normal		
Picture freeze	Yes		
Multi picture : PIP (AV)/POP (AV)	No		
Dynamic Backlight Control	Yes (according to the picture showing)		
LED Backlight	/		
Deinterlacer (No/linear/motion adaptive/motion compensative)	3D motion adaptive		
Film mode / reverse 3:2/2:2 pull down	Yes / Yes		
Full HD support (1080P)	Yes		
Single scan / Dual scan (120HZ)	Single Scan		
Zoom type : 4/3 format	Yes		
Zoom type : 14/9 Zoom	Yes		
Zoom type : 16/9 Zoom	16/9 ZOOM 1		
Zoom type : 16/9 Zoom up/down	16/9 ZOOM 2		
Zoom type : Cinerama	Yes		
Zoom type : 16/9 Format	Yes		
Zoom type : Auto (by SCART Pin8 and WSS)	No		
Picture Auto adjustment (PC mode)	Yes		
Sound			
Sound type (Mono/AV stereo/Stereo)	AV stereo		
Music Power (Watt)/RMS Power (Watt)	8W + 8W		
Tone control (Bass&Treble / Graphic Equalizer)	Bass&Treble		
Special sound effect (AVL / WIDE / Pseudo /...)	AVL		
Surround system (Dolby / VD / SRS / BBE / ...)	Built-in Surround		
Sound control (Volume , Balance , Mute)	Volume, Balance, Mute		
Sound presets (User/Speech/News/Standard)	Standard / Music / Film / Voice / Personal		
Headphone volume control (Separated / linked)	Yes		
Sound quality (High / Mid / Low)	Balance, Tone, EQ, Virtual Surround, Treble/Bass		
Reception and Decoding capability			
RF range (ATV)	FS/181CH		
RF range (DTV)	SATVD-T		
Built-in Power supply BOM Costing Target	IEC		
Color System (PAL/SECAM/NTSC/PAL M,N)	NTSC/PAL		
Audio Standard (B/G/H/D/K/K'/L/L')	M/N		

Stereo audio system (Nicam,MTS,A2,...)	BTSC
Video standard NTSC 3.58 / 4.43 (AV)/PAL 60	Yes
DTV SD support (DVB-T/S/C , ATSC , QAM , ...)	ISDB-T
DTV HD Support	H.264
MPEG5	No
HD capability with YPbPr	Yes (720p; 1080i; 1080p@24/50/60Hz; 480i/p; 576i/p)
Frame Rate	24/25/30/50/60 Hz
PC capability (up to maximum format)	Up to 1280X1024 60Hz
HDMI capability (AV/PC Format)	Up to 1080P 24/50/60HZ
Compatible video format if DVD/USB: DivX/VCD/SVCD/JPEG/AVI/MPEG2/WMV- HD/SD	JPEG/MPEG2/MPEG4/H.264/DivX (depending on license)
Compatible audio format if DVD/USB: MP3/WMA/AAC/MPEG1/...	MP3 / WMA (depending on license)
Playable Discs (CD/CD-R(RW)/CD-ROM/DVD+R/+RW/-R/-RW)	No
Card reader format compatibility	No
Macrovision	Yes
PVR	No (FOR USB)
Network	No
User convenience	
OSD Language*	English, French, Spanish, Portuguese
OSD Positioning	No
OSD Transparency Adjust	No
OSD Timeout Adjust	No
Customer Brand name(LOGO)	Yes
IB languages	English
ATV Program Numbers (example: 99+3AV input)	181+9AV
DTV Program Numbers	
Program edit (naming , sorting , skip , swap)	Naming / Skip / Swap
Auto Naming/Auto Sorting	No
TV Guide(DTV EPG)	EPG
Favorite program	Yes
Number of buttons on cabinet (Power; Vol+/-; Pr+/-, Menu)	CH+, CH-, VOL+, VOL-, INPUT, MENU
Main switch button (Yes/No)	No
CCD (Closed Caption)/V-CHIP	Yes/Yes
Text Standard: (Top, FLOF,...)	No
Teletext Level: 2.5 / 1.5	No
Pages for teletext	No
Teletext character sets ****	No
DVB-T teletext	No
Real clock	From DTV
Sleep timer	15-120 Min.
Timer	Turn On / Off, Program Switch
Parent Control -Source and Channel lock (Input code for certain)	No
Parent Control - Child lock (set the lock of the keyboard, only the RCU can control the TV)	No
Parent Control - Kid pass (preset the ontime, channel for each)	No
Parent Control - Channel lock (For digital transmission and DVD program, to filter some programmes)	No
Calendar / Games	No
No program auto switch off	15 mins.
Hotel mode (Y/N)	Optional
DVD player (No/slot/tray)	No
Tuner FM (yes/no)	No
software download(RS232/CI/USB/OAD)	USB
Factory reset	Yes (Preset LOGO and OSD Language/Preset Standard Picture,color,sound,Volume/Close MP3/DivX/RMVB/MP4)
Quick view	Yes (For going back to previous channel. For example, original you are watching CH1, and then you switch to CH3, and then you switch to CH5, then you press "Quick View", will jump back to CH3, and you press "Quick View" again, will jump back to CH5. This function is not workable on HDMI, AV those sources, only for RF.)
Screen saver	Yes
Blue Back	Yes
LED indicator(Power on/Standby)	Green (or Blue) / Red
Connectors -Rear	
RF Input (Antenna): <i>Air/ Cable/ 2in1</i>	1 tuner with 2 terminals
Scart : CVBS in&out / RGB / S-VIDEO	No
CINCH video in / out (AV1)	1 x AV IN, 1 x AV OUT (RCA)
CINCH audio in / out (two volume control on Audio out/can be used 2 times)	1 x AV IN, 1 x AV OUT (RCA)
S-video in	No

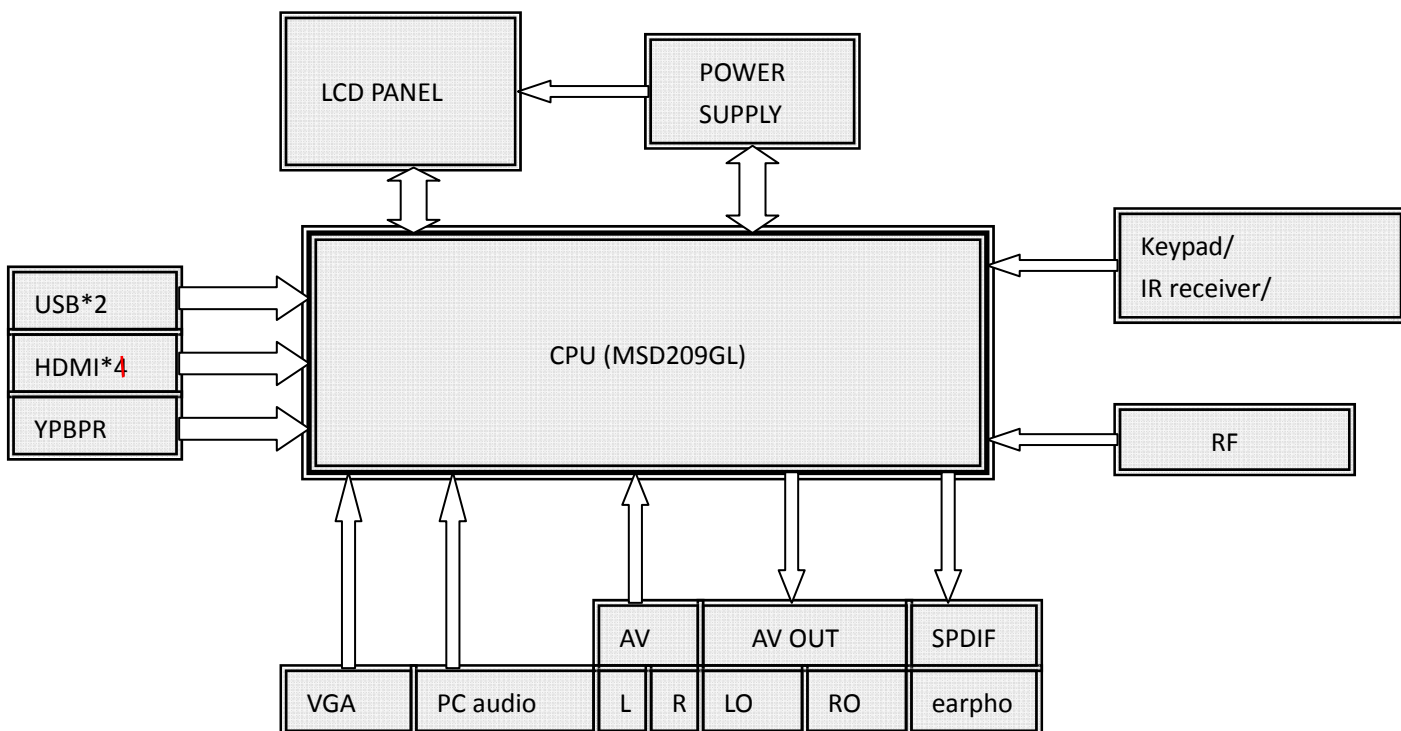
Component Video Input (YCrCb/YPrPb)	1 (RCA)		
Component Audio Input (YCrCb/YPrPb)	1 (RCA)		
VGA in / Audio L/R in / Jack audio in 3.5mm	1 VGA, 1 Audio IN for VGA		
HDMI	2 (version 1.3)		
DVI	NO		
Audio input for DVI	NO		
CINCH subwoofer out / Coaxial out (S/PDIF)	NO		
Headphone output connector (mm)	NO		
RS232 (Y/N , VGA or DB9 port ...)	NO		
Card Readers	NO		
USB slot (No/1.1/2)	NO		
DVB-CI (common interface)	NO		
External power converter input	NO		
Connectors -Side			
HDMI	1 (version 1.3)		
AV-IN	1		
AV-OUT	NO		
Component Video Input (YCrCb/YPrPb)	NO		
Component Audio Input (YCrCb/YPrPb)	NO		
Headphone output connector (dia.mm)	1 (3.5mm)		
USB slot (No/1.1/2)	2 (Software update, JPEG, MP3, WMA, RMVB, DivX) Multimedia depends on license Both USB 2.0, and both provide 1A Power Current, can support 2.5" Mobile HDD.		
DLNA	No		
UI/RC			
UI design (font/pixel, 2D/3D graphic engine..)	SOD Standard		
RC Model	RGB Standard		
RC system	RGB Standard		
RC # of keys			
Accessories included			
Carton (English/French/Spanish)	English		
IB	English		
Circuit diagram	Yes		
Batteries	Yes		
Product registration Card	Yes (English)		
AC power cords	Optional		
AC Cable Length	1.8m		
Audio Cord (Jack 3.5mm)	No		
VGA Cord	No		
Wallmount frame	Optional		
Antenna Cable	No		
General Data			
Size (W x H x D, with stand) in mm	-		
Size (W x H x D, without stand) in mm	-		
Package Size (W x H x D, without stand) in mm	-		
Net Weight in kg	-		
Gross Weight in Kg	-		
Design / Mechanical			
Wallmount VESA compatible (standard reference)	Yes		
Adaptor for VESA wallmount compatibility (accessory ref)	Yes		
Desktop Stand (included/optionnal + ref/No)	included		
Panel Tilt (Fowards/Backwards/Rotation)	No		
Swivel function desktop stand (yes/No) + motorized?	No		
Docking station (yes/No)	No		
Floor Stand (included/optionnal + ref/No)	No		
Glass shield (yes/No)	No		
Finish on Front	-		
Finish on side	-		
Finish on back	-		
Finish on stand	-		
number of colors on carton box	2		
Brand logo	Customer Inlet		
Other logo	No		
External AC/DC Power with DC power cord (yes/No)	No		
Handle (yes/No)	No		
Detachable speaker (yes/No)	No		
Rating Label langages	English		

2 Circuit Diagram

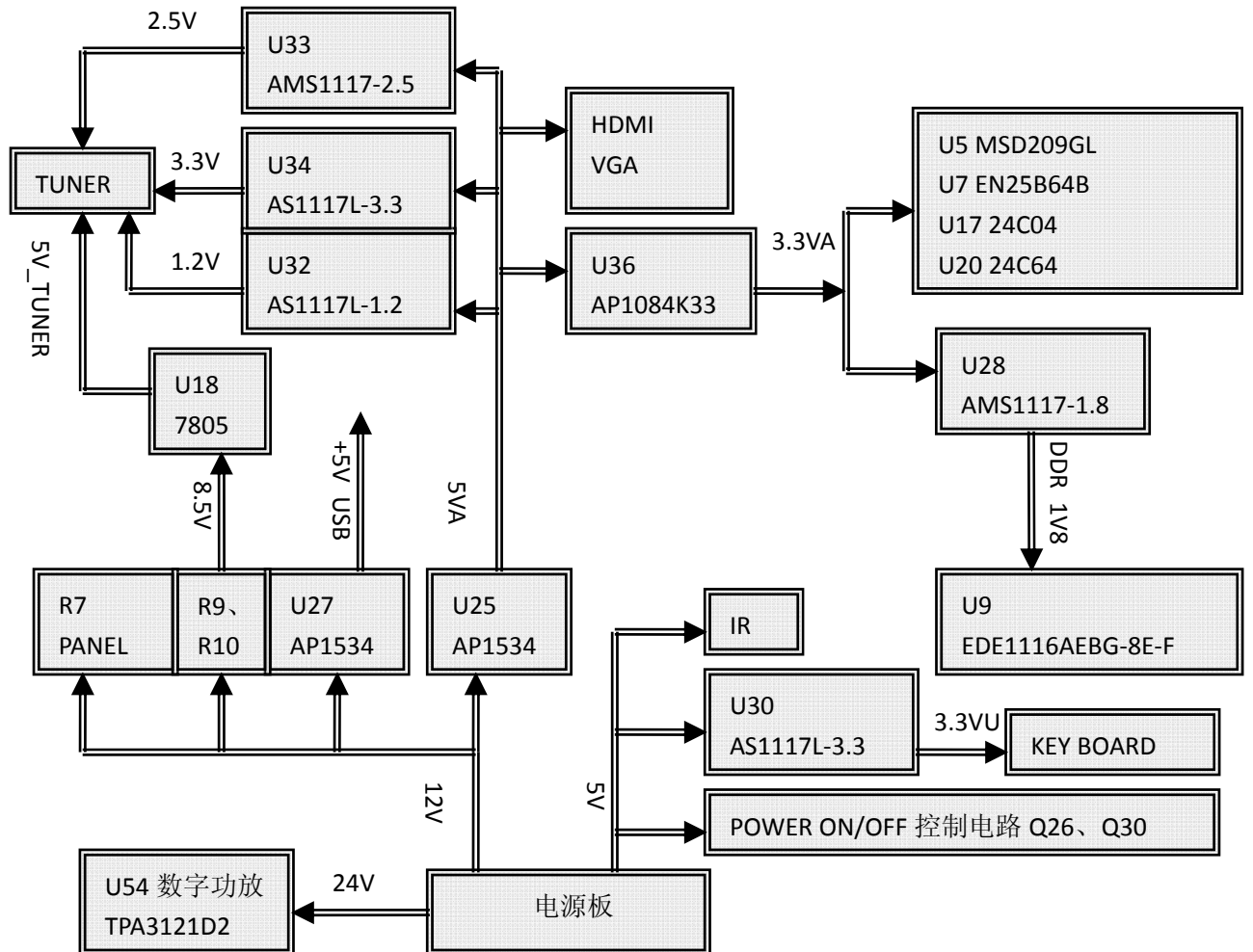
See the supplement

3. Signal Flow Graph

3.1 Chassis signal flow graph



3.2 Power flow graph chart



4 IC Datasheet

4.1 MSD209GL

4.1.1 General Description

The MSD209GL is a highly integrated controller IC for LCD/PDP DTV applications with resolutions up to full-HD(1920X1080). It is configured with an integrated triple-ADC/PLL, a multi-standard TV video and audio decoder, a motion adaptive video de-interlacer, a scaling engine, the MStarACE-3 color engine, an advanced 2D graphics engine, a transport processor, a high-definition(HD) MPEG video decoder, a high-definition(HD)H.264 video decoder, a RealVideo decoder, a JPEG video decoder, a MPEG-4 decoder, and a 24-bit DSP for MPEG audio decoding, a DVI/HDCP/HDMI receiver, and a peripheral control unit providing a variety of HDTV control functions.

For digital TV application, the MSD209GL comprises an MPEG-2 transport processor with advanced section filtering capability, an MPEG-2 (MP@HL profile) video decoder, a MPEG-4 decoder, a H.264 video decoder, and an audio DSP decoder for MPEG audio streams, MPEG layer I and II digital audio decoder with analog audio outputs that are designed to support existing and future DVB-T programs while handling conditional access. Furthermore, it is also possible to decode JPEG, RealVideo streams, and MP3 formats from external sources such as USB interface.

For analog TV, the MSD209GL includes NTSC/PAL/SECAM multi-standard video decoder comprising a 3D motion adaptive comb filter and time-based correction, and a NICAM/A2 audio decoder to support worldwide television standards. The MSD209GL is also configured with a VBI processor to decode digital information such as Close Caption/V-chip/teletext/WSS/CGMS-A/VPS. In addition, the MStar advanced LCD TV processor enhances video quality, motion adaptive de-interlacer, picture quality adjustment units, and MStarACE-3 color engine.

With USB 2.0 host controllers, UART, IR, SPI, I2C, and PWM, the MSD209GL fulfills all requirements in advanced DTV sets. To reduce system costs, the MSD209GL also integrates intelligent power management control capability for green-mode requirements and spread-spectrum supports for EMI management.

U5A



4.2.1 Description

The TPA3121D2 is a 15-W (per channel), efficient,

Required) class-D audio power amplifier for driving stereo speakers in a single-ended configuration or a mono

- **Single-Ended Analog Inputs** speaker in a bridge-tied-load configuration. The

- **Thermal and Short-Circuit Protection With** TPA3121D2 can drive stereo speakers as low as 4 Ω .

Auto Recovery The efficiency of the TPA3121D2 eliminates the need

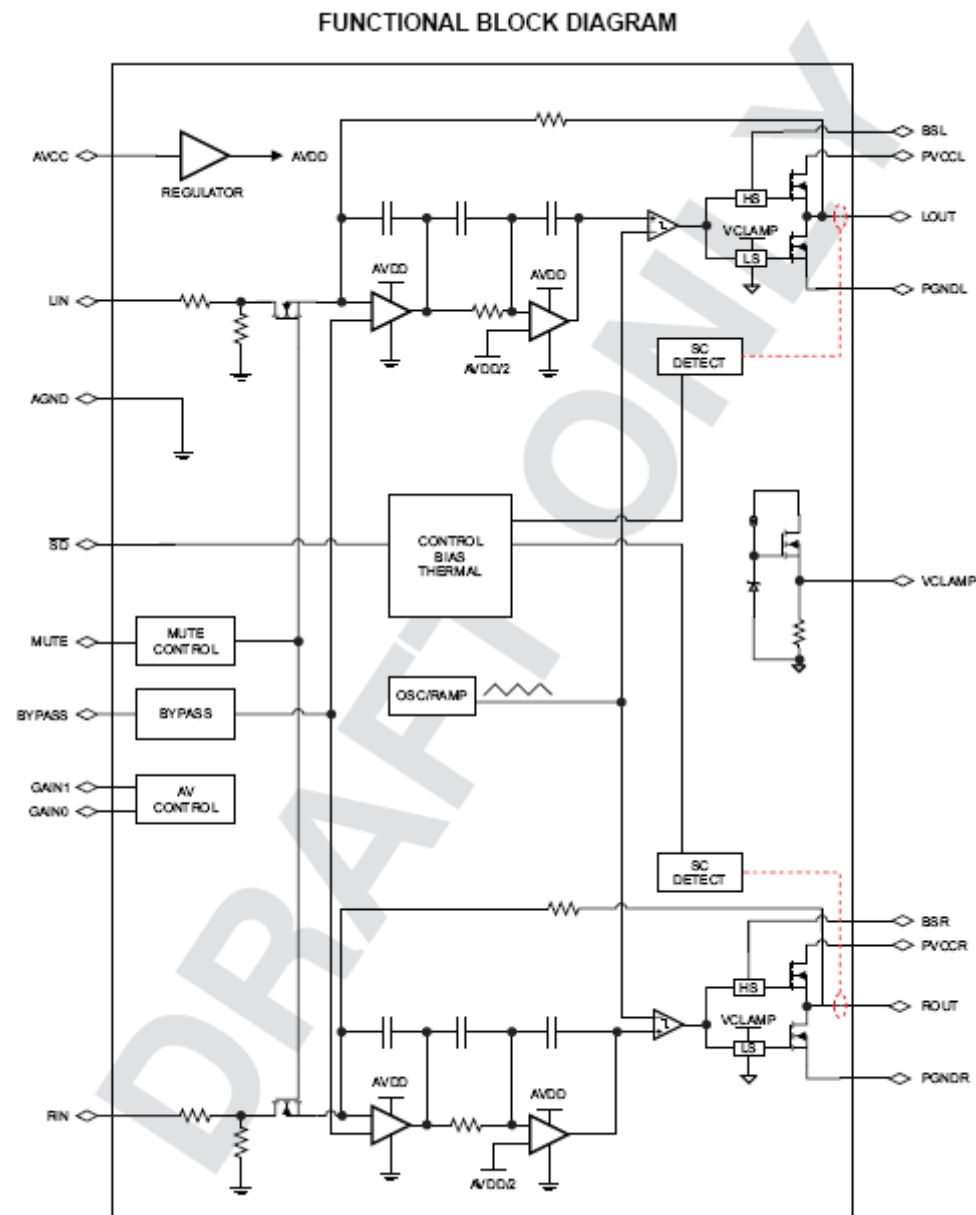
- **Space-Saving Surface Mount 24-Pin TSSOP** for an external heat sink when playing music.

Package The gain of the amplifier is controlled by two gain

- **Advanced Power-Off Pop Reduction** select pins. The gain selections are 20, 26, 32, and 36 dB.

The patented start-up and shutdown sequences minimize pop noise in the speakers without additional circuitry

4.1.2 Internal Block Diagram



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4.1.3 Package and Pin



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

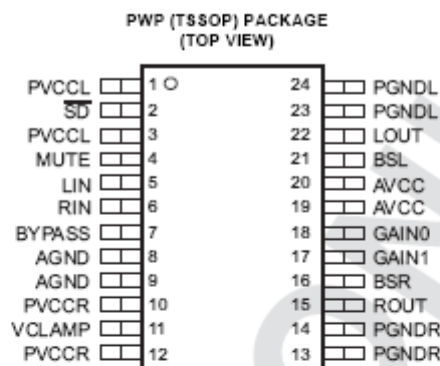


Table 1. TERMINAL FUNCTIONS

TERMINAL		I/O/P	DESCRIPTION
NAME	24-PIN (PWP)		
SD	2	I	Shutdown signal for IC (low = disabled, high = operational). TTL logic levels with compliance to AVCC
RIN	6	I	Audio Input for right channel
LIN	5	I	Audio Input for left channel
GAIN0	18	I	Gain select least-significant bit. TTL logic levels with compliance to AVCC
GAIN1	17	I	Gain select most-significant bit. TTL logic levels with compliance to AVCC
MUTE	4	I	Mute signal for quick disable/enable of outputs (high = outputs switch at 50% duty cycle, low = outputs enabled). TTL logic levels with compliance to AVCC
BSL	21	I/O	Bootstrap I/O for left channel
PVCCCL	1, 3	P	Power supply for left-channel H-bridge, not internally connected to PVCCR or AVCC
LOUT	22	O	Class-D 1/2-H-bridge positive output for left channel
PGNDL	23, 24	P	Power ground for left-channel H-bridge
VCLAMP	11	P	Internally generated voltage supply for bootstrap capacitors
BSR	16	I/O	Bootstrap I/O for right channel
ROUT	15	O	Class-D 1/2-H-bridge negative output for right channel
PGNDR	13, 14	P	Power ground for right-channel H-bridge.
PVCCR	10, 12	P	Power supply for right-channel H-bridge, not connected to PVCCCL or AVCC
AGND	9	P	Analog ground for digital/analog cells in core
AGND	8	P	Analog ground for analog cells in core
BYPASS	7	O	Reference for preamplifier inputs. Nominally equal to AVCC/8. Also controls start-up time via external capacitor sizing.
AVCC	19, 20	P	High-voltage analog power supply. Not internally connected to PVCCR or PVCCCL
Thermal pad	Die pad	P	Connect to ground. Thermal pad should be soldered down on all applications to secure the device properly to the printed wiring board.

4.2 TUNER VA1G5BF8015

4.2.1 Tuner VA1G5BF8015 description

1、Receiving frequency range:
54MHz to 864MHz (Lower boundary to Higher boundary)

VHF Low Band : 54 ~ 160.99 MHz

VHF High Band: 161 ~ 425.99 MHz

UHF Band: 426 \sim 864 MHz

2、Receiving system

Analog: NTSC, PAL-M, Digital: ISDB-T

3、RF input impedance:

75 Ω Unbalance

4、Load impedance

VIDEO OUT:10K Ω Load

SIF OUT: 47K Ω Load

1.7 Intermediate frequency:

Analog

Picture carrier 45.75MHz

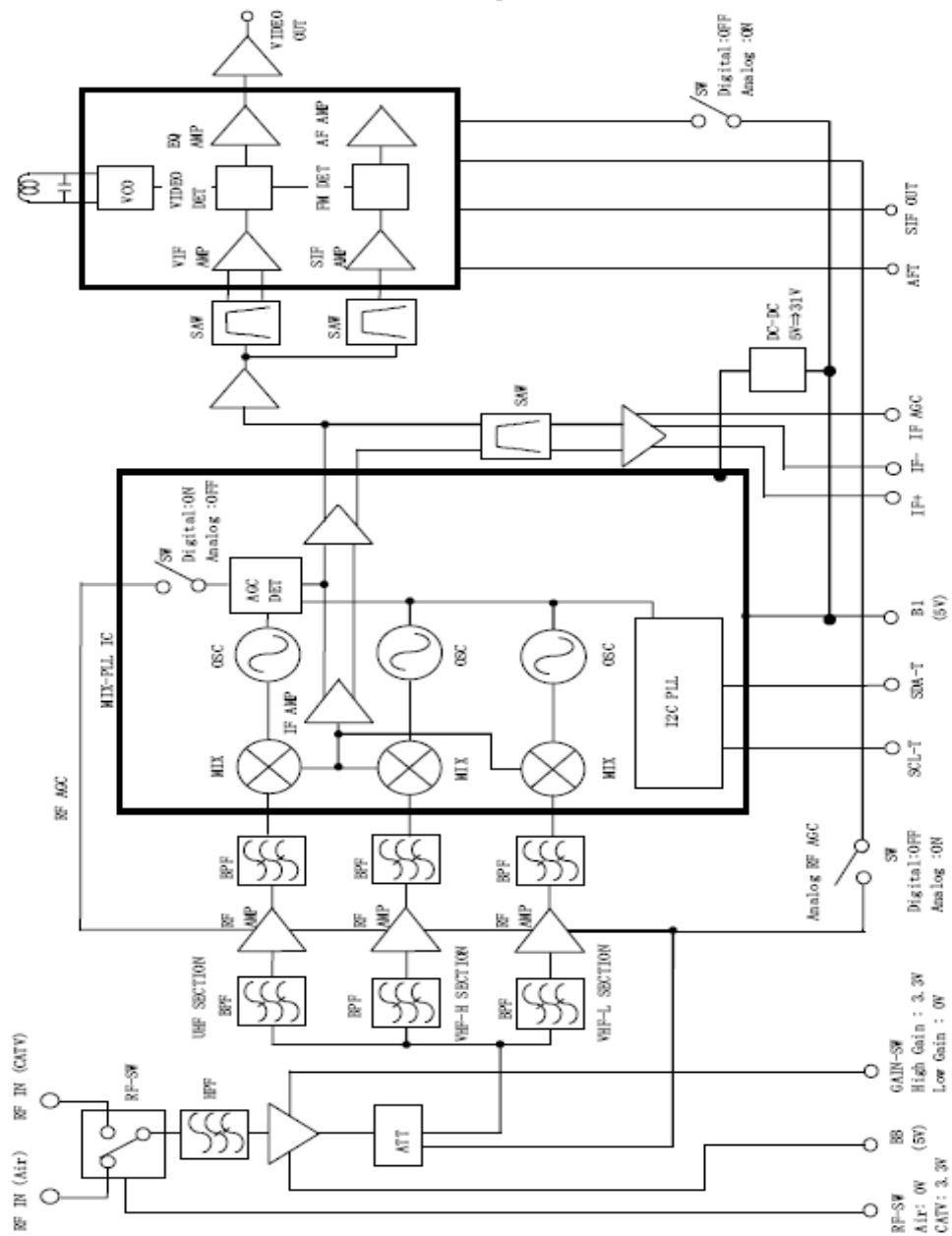
Sound carrier 41.25MHz

Digital

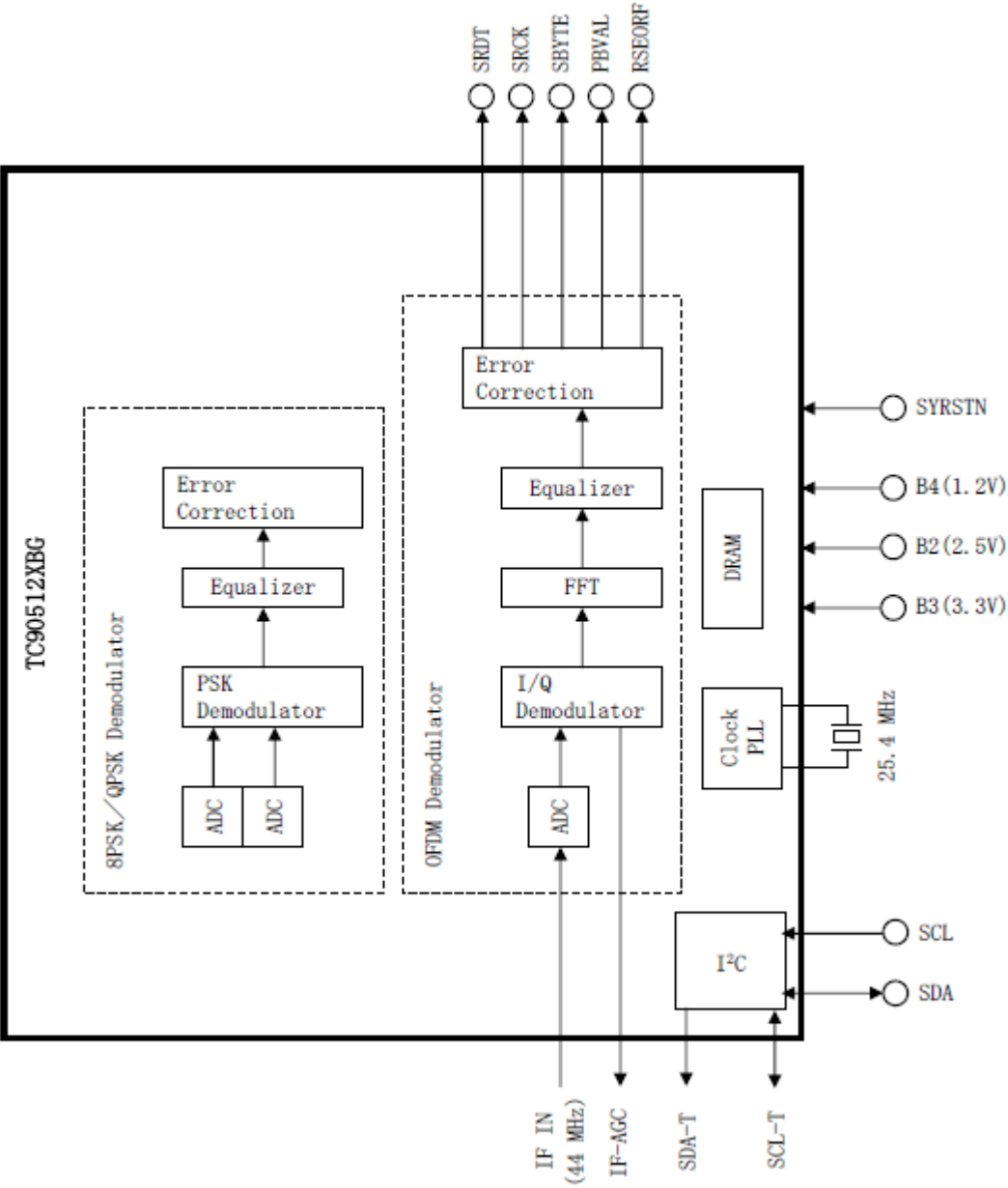
Center Frequency 44MHz

4.2.2 Block Diagram

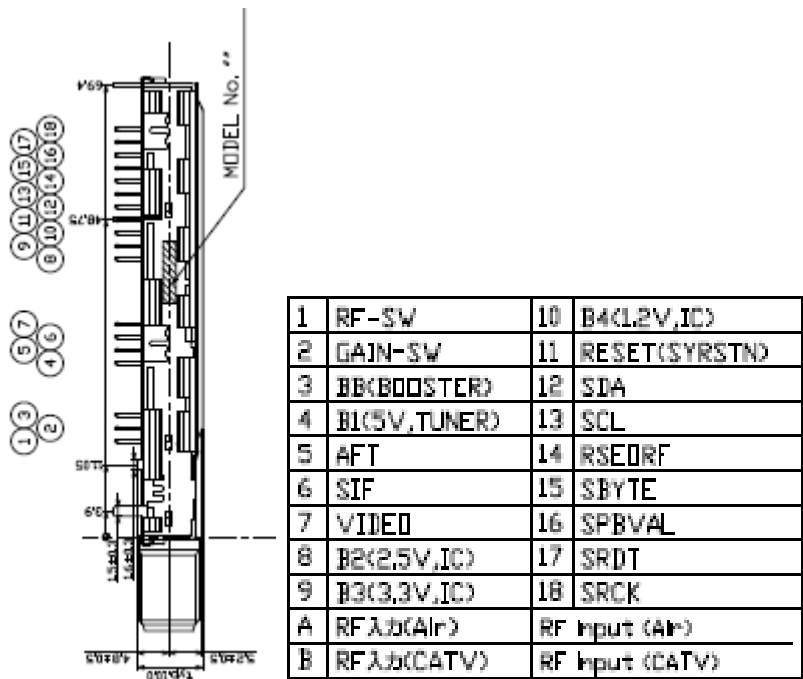
RF-IF Block diagram



De-Modulator part



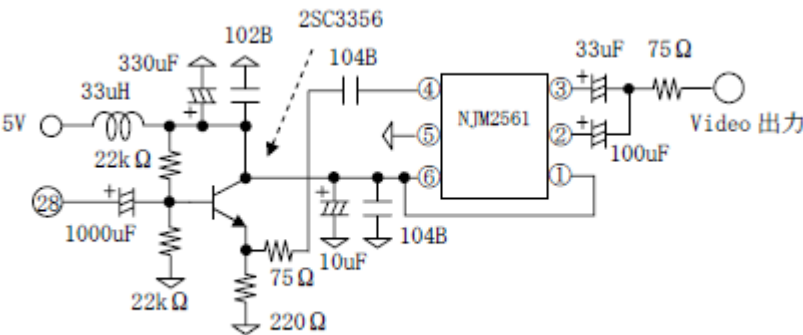
4.2.3 Terminal



Terminal and function

4.2.4 Major terminal operation voltage

Terminal	operation voltage
1. RF-SW	3.3V
2. GAIN-SW	3.3V
3. BB	5V
4. B1	5V
8. B2	2.5V
9. B3	3.3
10. B4	1.2V



Video output circuit

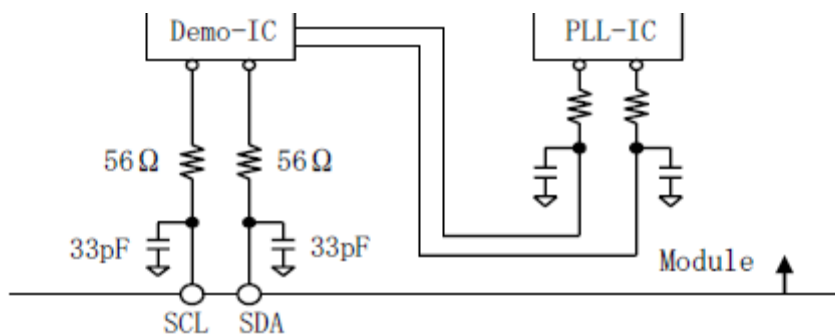


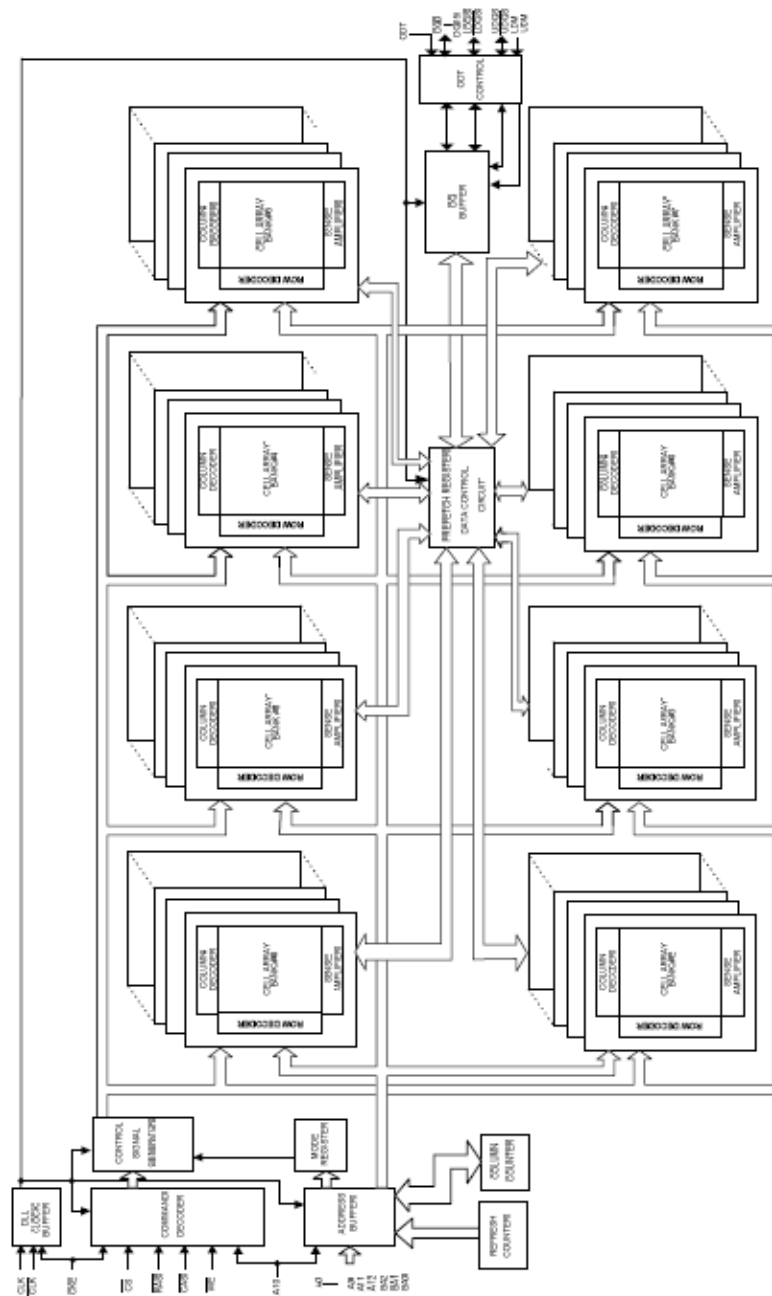
图 3 I2C interface

4.3 DDR2 SDRAM: **W971GG6JB** (U9)

4.3.1 GENERAL DESCRIPTION

The W971GG6JB is a 1G bits DDR2 SDRAM, organized as 8,388,608 words 8 banks 16 bits. This device achieves high speed transfer rates up to 1066Mb/sec/pin (DDR2-1066) for general applications.。

4.3.2 BLOCK DIAGRAM



NOTE: The cell array configuration is 8192 x 1024 x 16

4.3.3 BALL CONFIGURATION

1	2	3	4	5	6	7	8	9
VDD	NC	VSS		A		VSSQ	$\overline{\text{UDQS}}$	VDDQ
DQ14	VSSQ	UDM		B		UDQS	VSSQ	DQ15
VDDQ	DQ9	VDDQ		C		VDDQ	DQ8	VDDQ
DQ12	VSSQ	DQ11		D		DQ10	VSSQ	DQ13
VDD	NC	VSS		E		VSSQ	$\overline{\text{LDQS}}$	VDDQ
DQ6	VSSQ	LDM		F		LDQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ		G		VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3		H		DQ2	VSSQ	DQ5
VDDL	VREF	VSS		J		VSSDL	CLK	VDD
	CKE	$\overline{\text{WE}}$		K		$\overline{\text{RAS}}$	$\overline{\text{CLK}}$	ODT
BA2	BA0	BA1		L		$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
	A10/AP	A1		M		A2	A0	VDD
VSS	A3	A5		N		A6	A4	
	A7	A9		P		A11	A8	VSS
VDD	A12	NC		R		NC	NC	

Pin name	Function	Pin name	Function
A0 to A13	Address inputs	ODT	ODT control
BA0, BA1, BA2	Bank select	VDD	Supply voltage for internal circuit
DQ0 to DQ15	Data input/output	VSS	Ground for internal circuit
DQS, /DQS, UDQS, /UDQS, LDQS, /LDQS	Differential data strobe	VDDQ	Supply voltage for DQ circuit
RDQS, /RDQS	Differential data strobe for read	VSSQ	Ground for DQ circuit
/CS	Chip select	VREF	Input reference voltage
/RAS, /CAS, /WE	Command input	VDDL	Supply voltage for DLL circuit
CKE	Clock enable	VSSDL	Ground for DLL circuit
CK, /CK	Differential clock input	NC ¹	No connection
DM, UDM, LDM	Write data mask	NU ²	Not usable

Notes: 1. Not internally connected with die.

2. Don't connect. Internally connected.

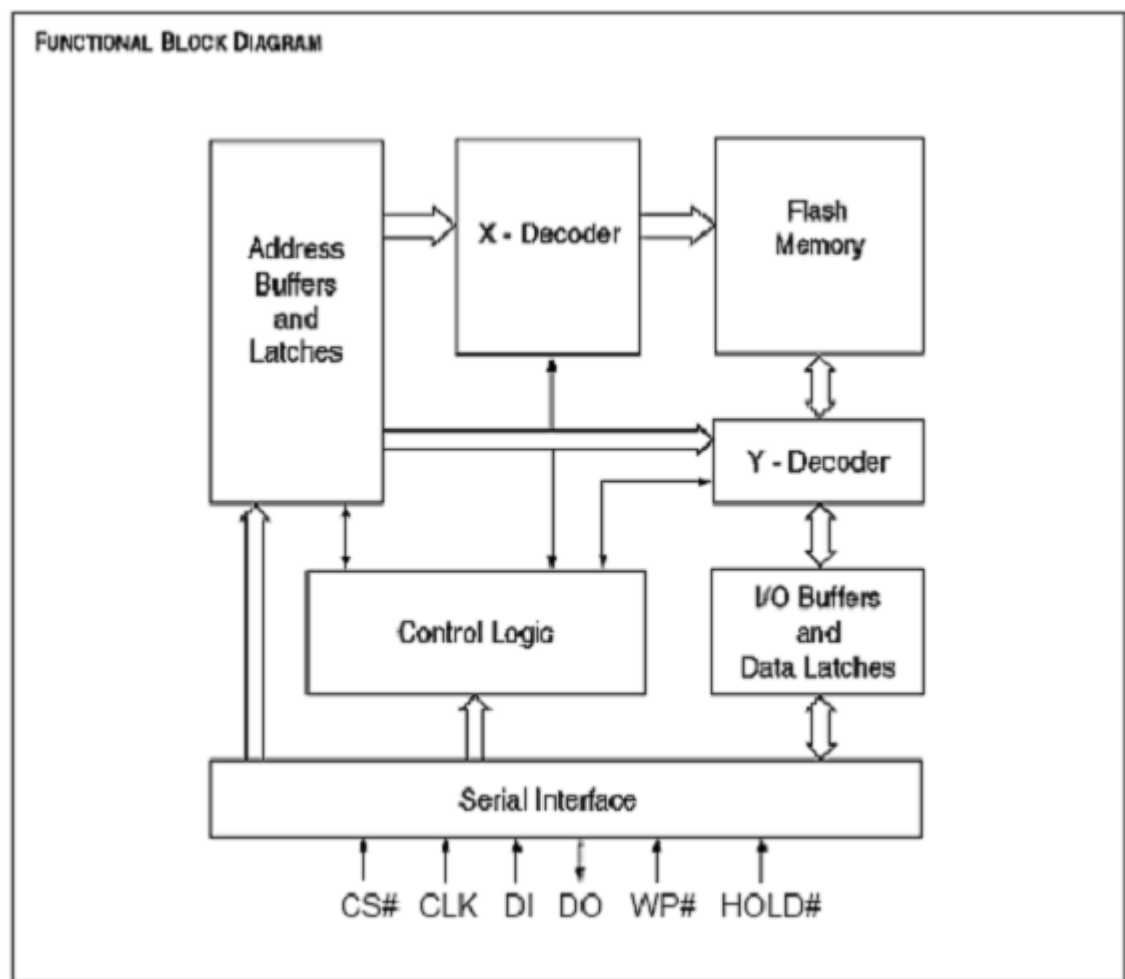
4.4 Program SPI FLASH: EN25B64-100FIP (U7)

4.4.1 *GENERAL DESCRIPTION*

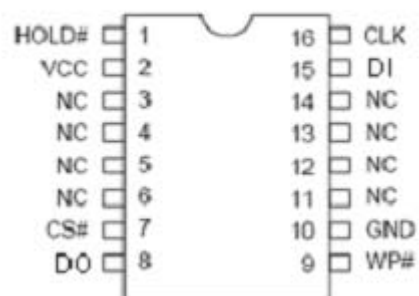
The EN25B64 is a 64M-bit (8192K-byte) Serial Flash memory, with advanced write protection mechanisms, accessed by a high speed SPI-compatible bus. The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction.

The EN25B64 has one hundred twenty-eight sectors including one hundred twenty-seven sectors of 64KB, one sector of 32KB, one sector of 16KB, one sector of 8KB and two sectors of 4KB. This device is designed to allow either single Sector at a time or full chip erase operation. The EN25B64 can protect boot code stored in the small sectors for either bottom or top boot configurations. The device can sustain a minimum of 100K program/erase cycles on each sector.

4. 5. 2 BLOCK DIAGRAM



4. 4. 3 CONNECTION DIAGRAMS



16 - LEAD SOP

Symbol	Pin Name
CLK	Serial Clock Input
DI	Serial Data Input
DO	Serial Data Output
CS#	Chip Enable
WP#	Write Protect
HOLD#	Hold Input
Vcc	Supply Voltage (2.7-3.6V)
Vss	Ground

PIN Names

4. 4. 4 SIGNAL DESCRIPTION

Serial Data Input (DI)

The SPI Serial Data Input (DI) pin provides a means for instructions, addresses and data to be serially written to (shifted into) the device. Data is latched on the rising edge of the Serial Clock (CLK) input pin.

Serial Data Output (DO)

The SPI Serial Data Output (DO) pin provides a means for data and status to be serially read from (shifted out of) the device. Data is shifted out on the falling edge of the Serial Clock (CLK) input pin.

Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Mode")

Chip Select (CS#)

The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high the device is deselected and the Serial Data Output (DO) pin is at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When CS# is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

Hold (HOLD#)

The HOLD pin allows the device to be paused while it is actively selected. When HOLD is brought low, while CS# is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don' t care). The hold function can be useful when multiple devices are sharing the same SPI signals.

Write Protect (WP#)

The Write Protect (WP#) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (BP0, BP1 and BP2) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected.

PCB Overview

See the supplement

6 Adjustment Instruction

6.1 Access the Factory Mode

1、 Access the Factory Mode :

Press source button first, then press 2, 5, 8, 0 one by one; press exit button or menu button to exit the factory mode.

3、 White balance adjustment:

a) Auto Adjust:

YUV source: input 576P 100% color bar signal, access factory menu and select the ADC item , AUTO ADC.

VGA source: input 800X600 chess signal, access factory menu and select the ADC item , AUTO ADC.

b) Manual adjustment:

Access the Factory Mode, select ADC item, press the left or right button to access the submenu.

- a) R Gain
- b) G Gain
- c) B Gain
- d) R Offset
- e) G Offset
- f) B Offset

Using the up or down button to select the item, and using the left or right button to adjust.

- | | |
|-------------------|--------------------------------|
| 4、 PANEL SETTING | setting the panel parameter. |
| 5、 SYSTEM SETTING | setting the system parameter. |
| 6、 SOURCE SETTING | setting the source parameter. |
| 7、 W/B ADJUST | setting the color temperature. |
| R Gain | |
| G Gain | |
| B Gain | |
| R Offset | |
| G Offset | |
| B Offset | |

- | | |
|------------------|-------------------------------------|
| 8、 PICTURE CURVE | setting the nonlinear picture curve |
|------------------|-------------------------------------|

9、PICTURE MODE setting the parameter of the presetting picture modes

10、SOUND NONLINEAR etting the nonlinear sound curve.

11、OTHER SETTING other setting items.

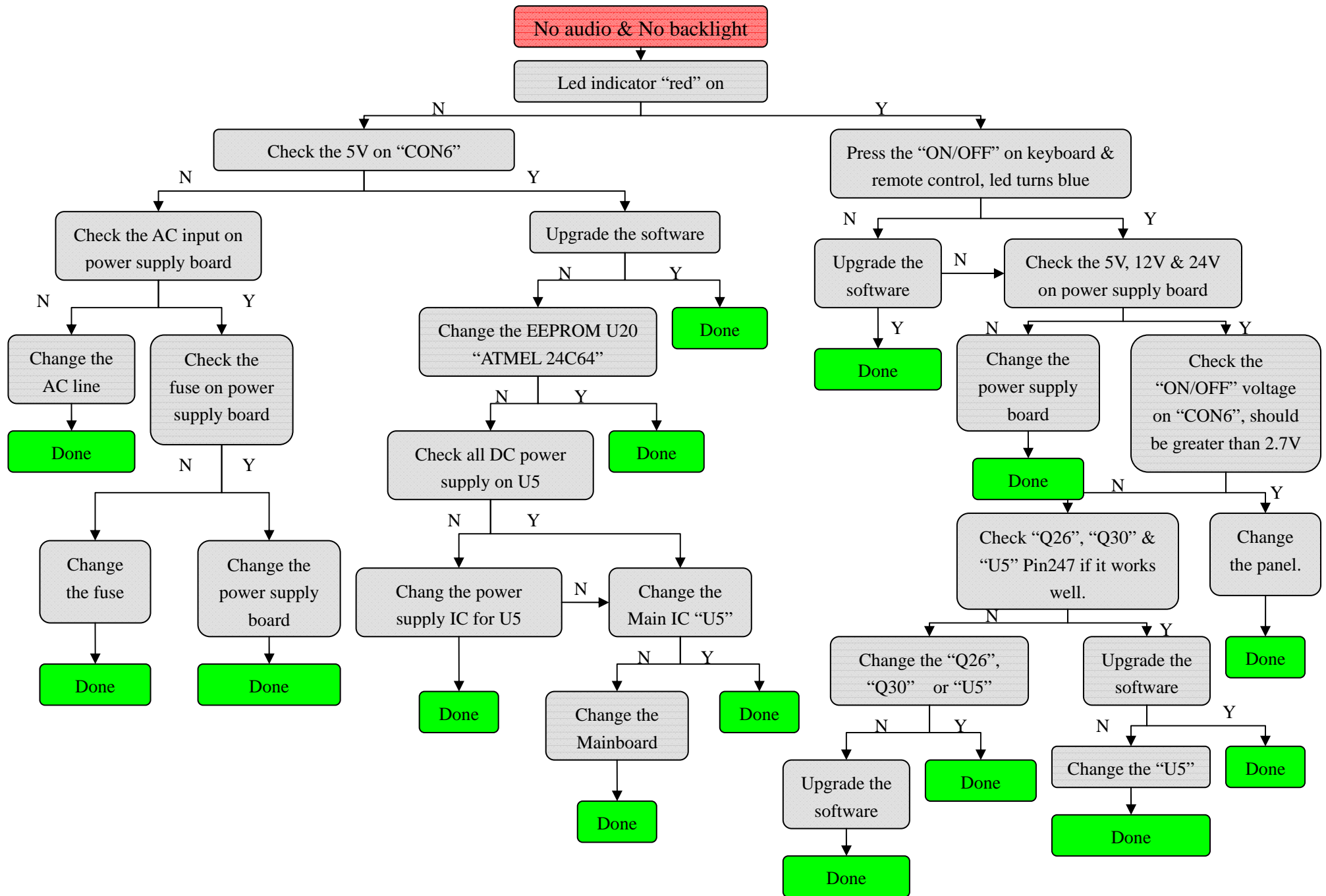
12、SW VERSION information of software version.

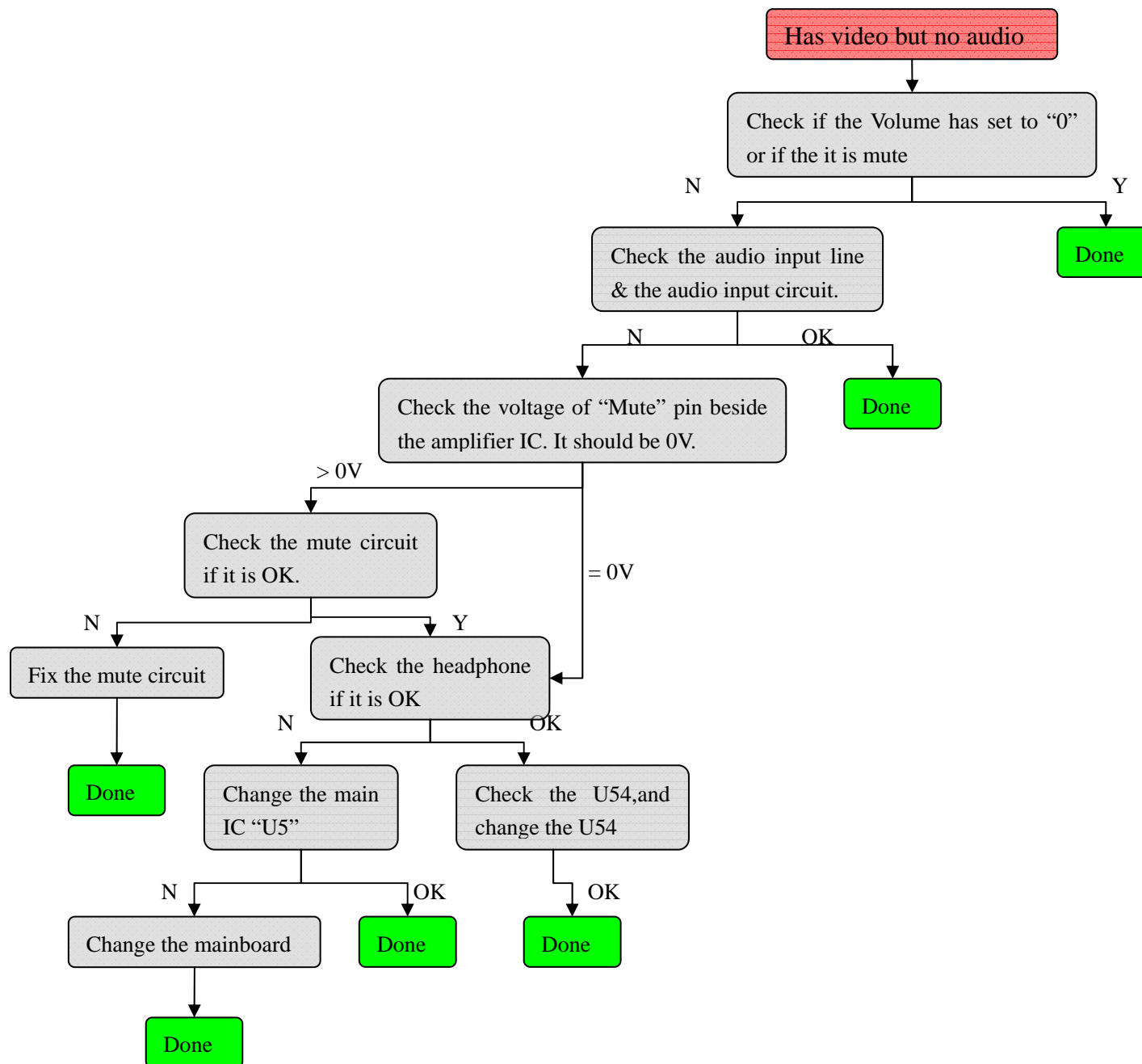
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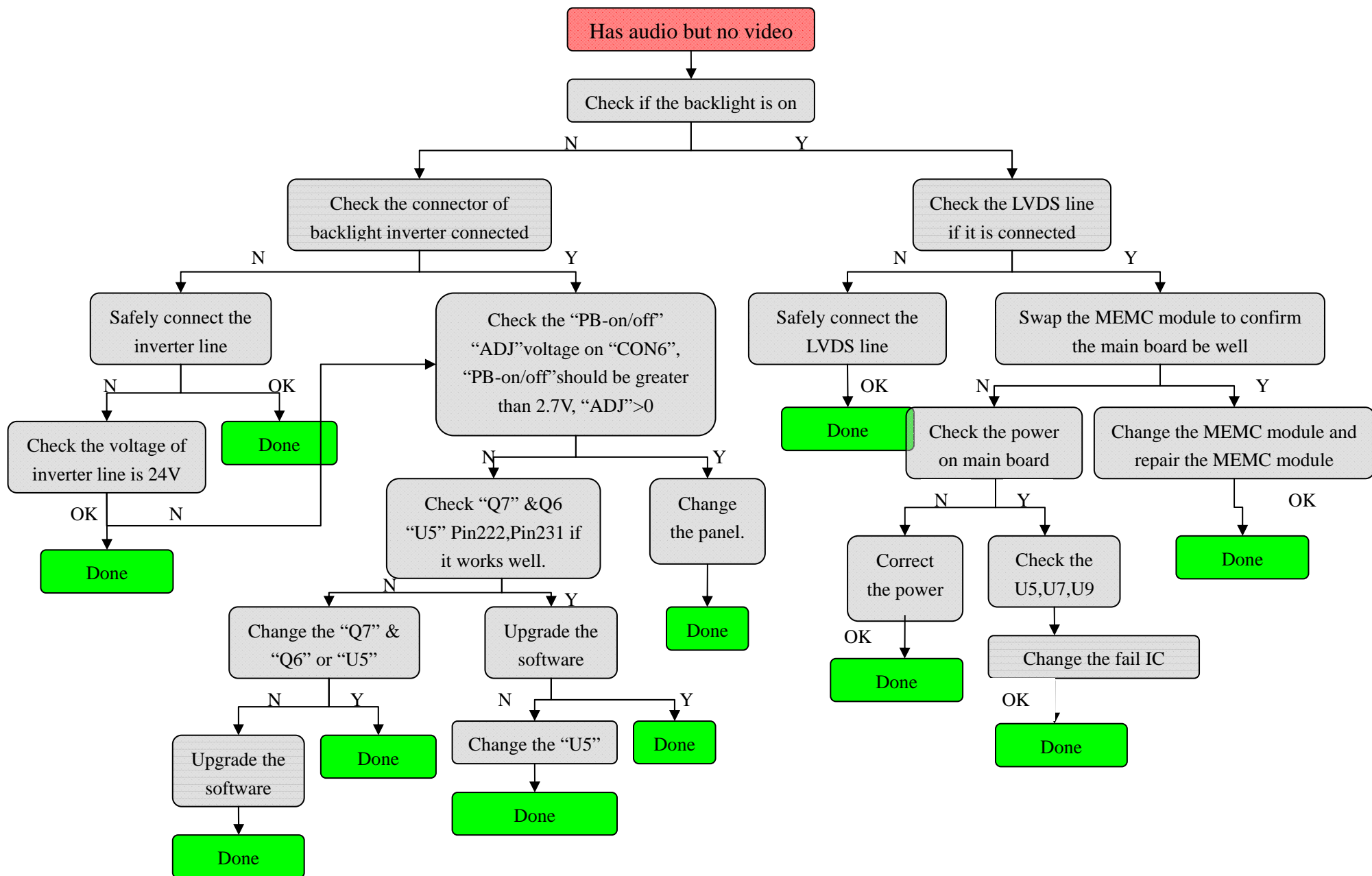
6.2 Upgrade the Software by USB port

- Copy the software file named merge.bin to the root directory of USB Disk ;
- Plug the USB Disk to the USB port of the LED;
- In TV or AV mode, press the Menu button and enter the Option page and select the last item Software Update(USB), then press OK or VOL+ button. Select the Yes item in the pop up menu and press OK button to start updating.
- After finished the update, the LED will restart.
- Please don' t switch off the LED during the updating process.

7 Typical failures



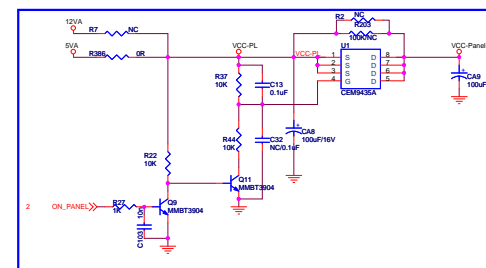
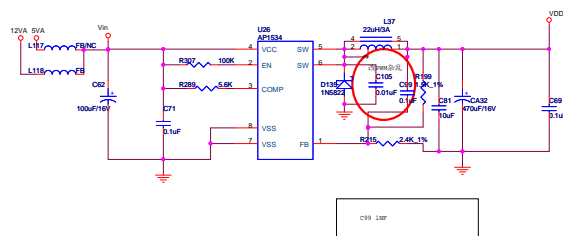
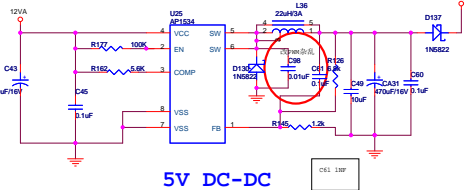




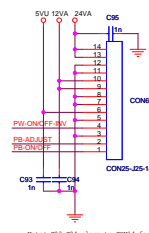
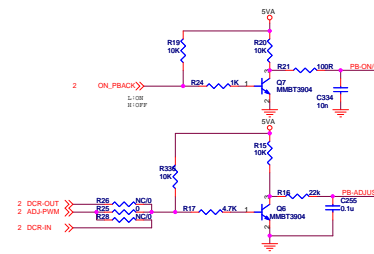
DC-DC Module

1.28V Main DC-DC

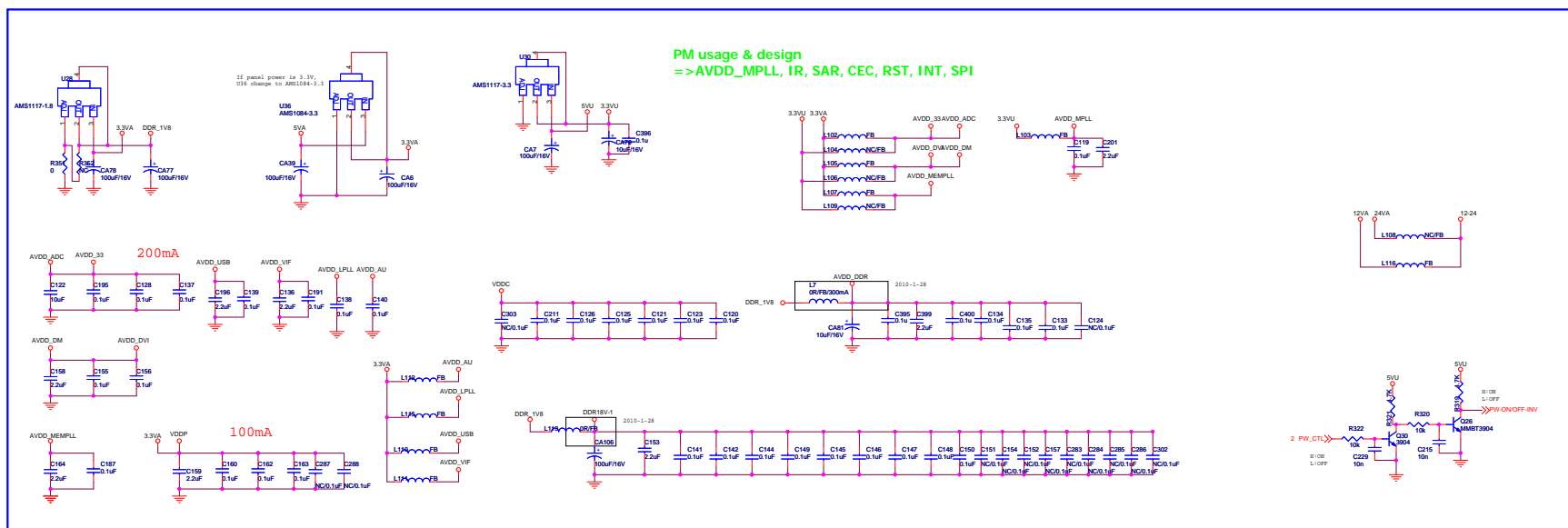
PANEL POWER



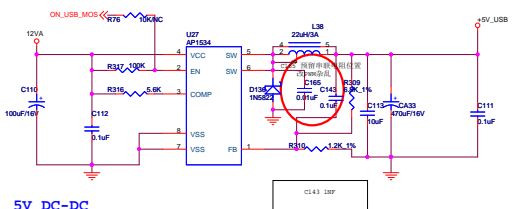
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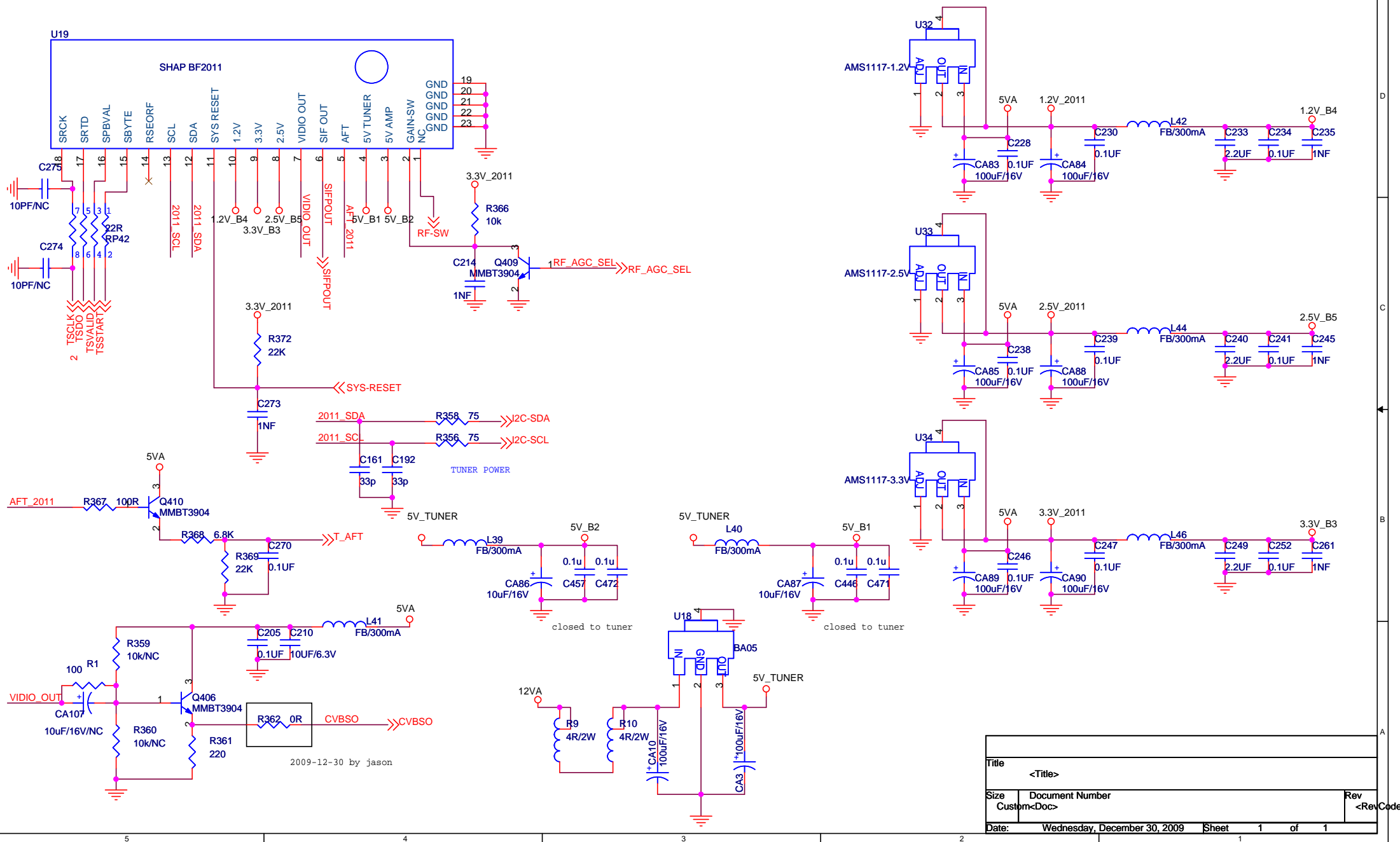
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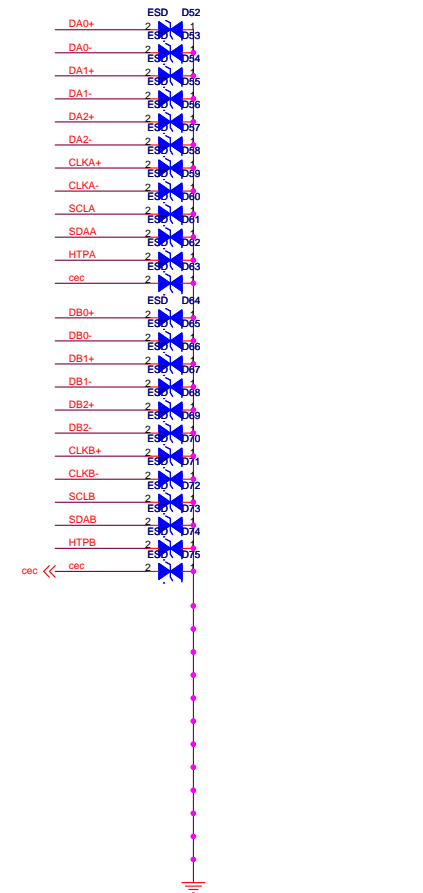
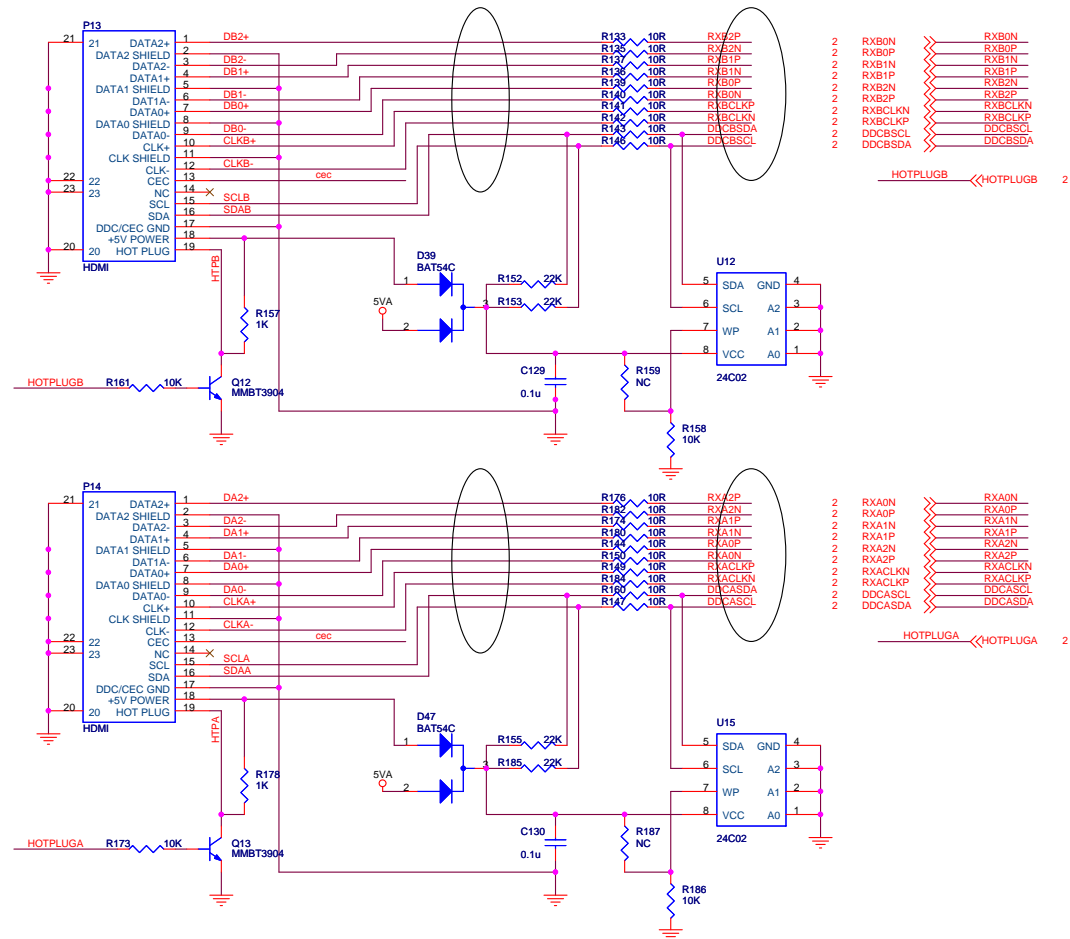
USB Power



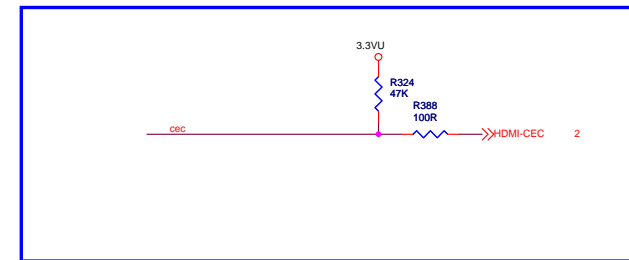
5V DC-DC

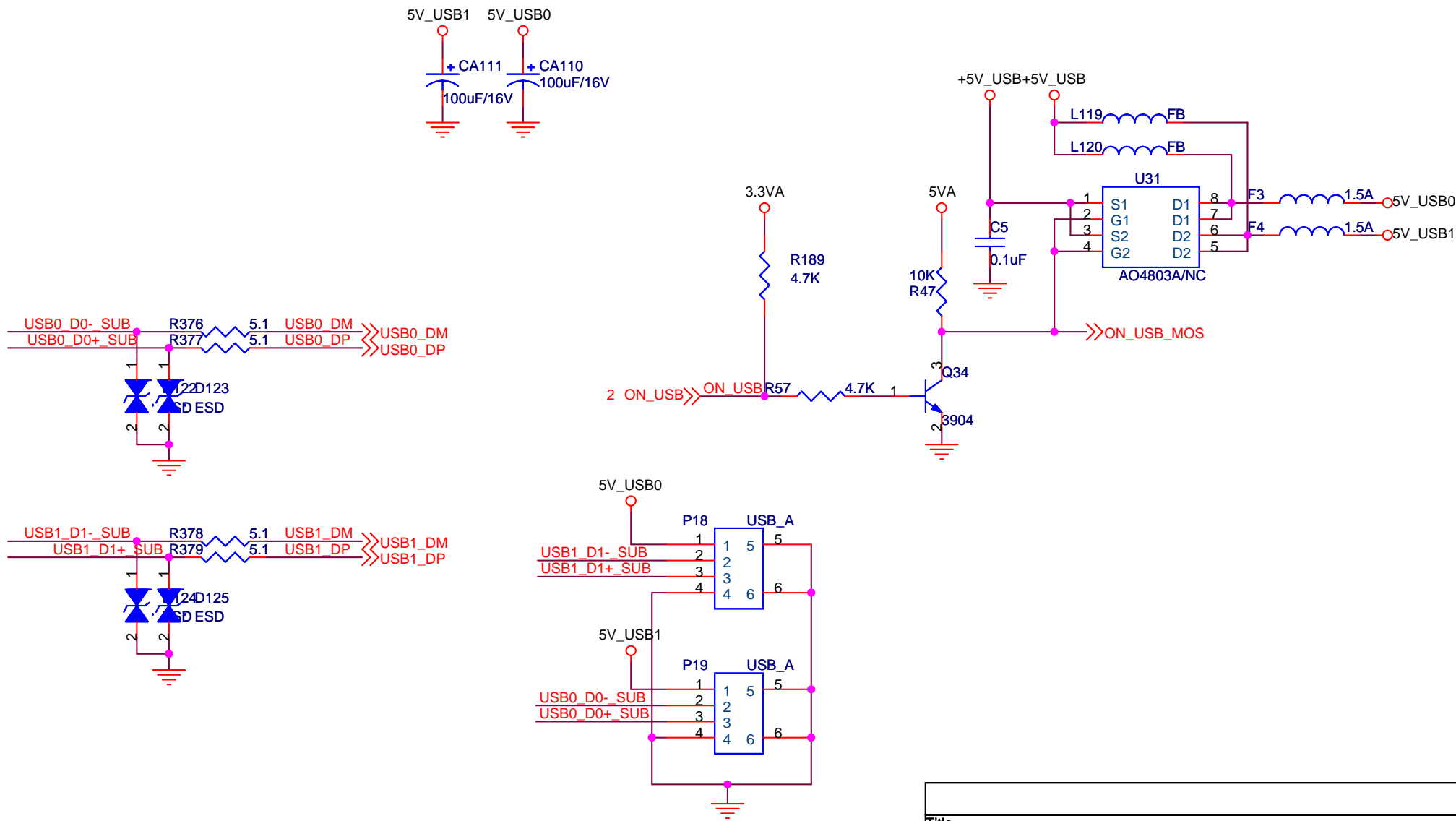


HDMI Input



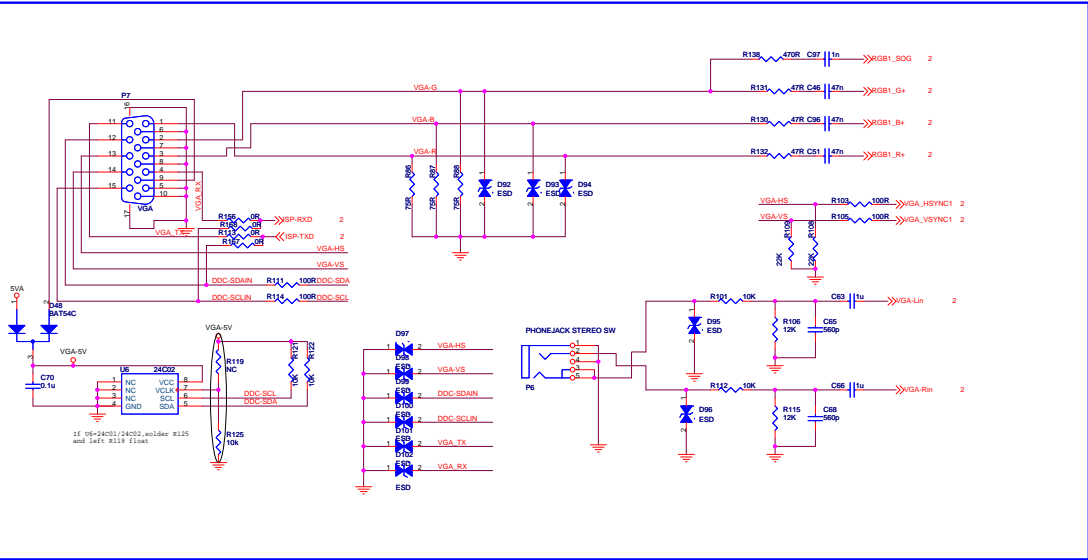
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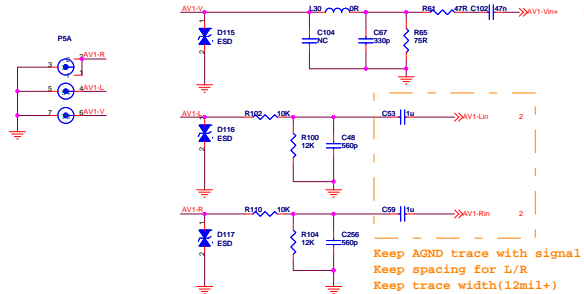


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VIF 256p demo Board		
Size	Document Number	Rev
Custom	USB	1.0
Date:	Thursday, November 12, 2009	Sheet 8 of 12

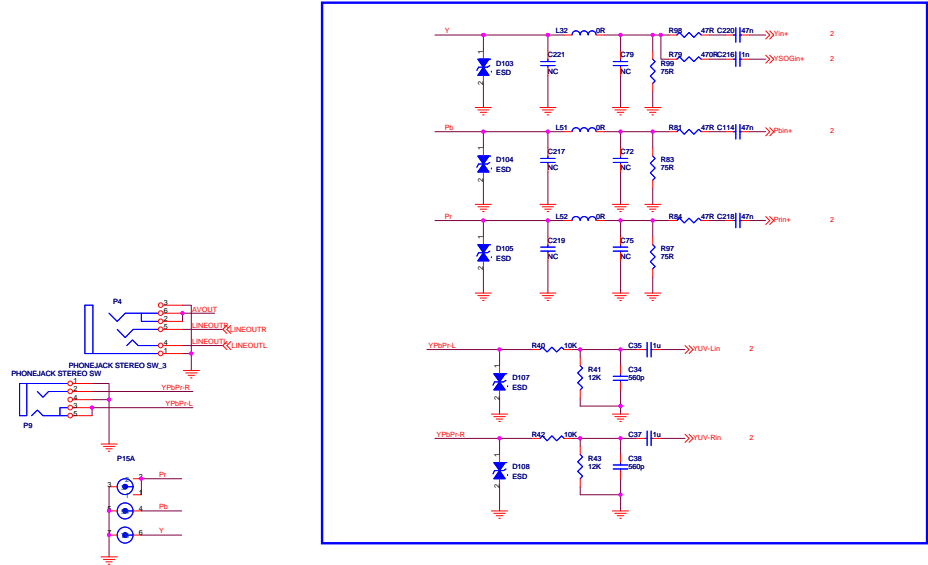
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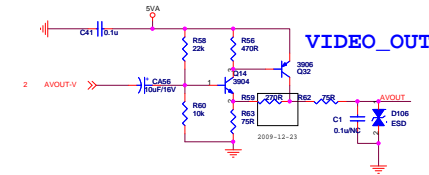
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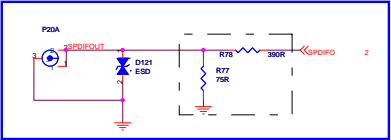
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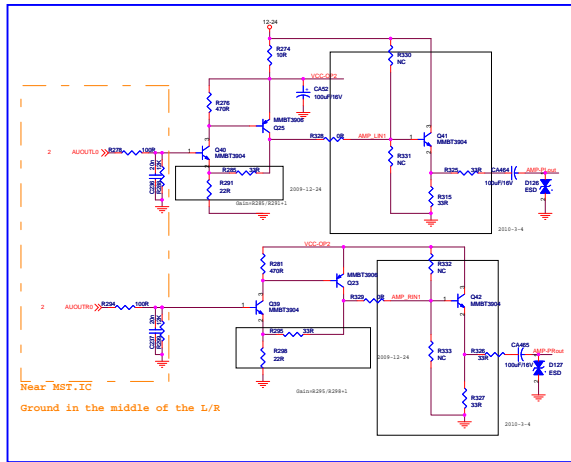
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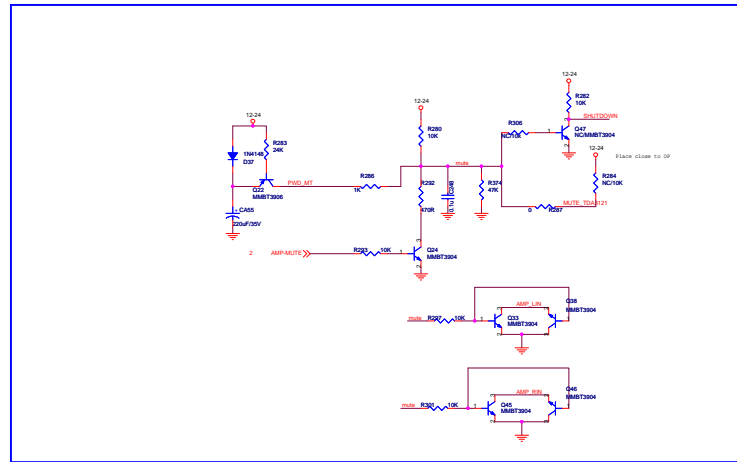
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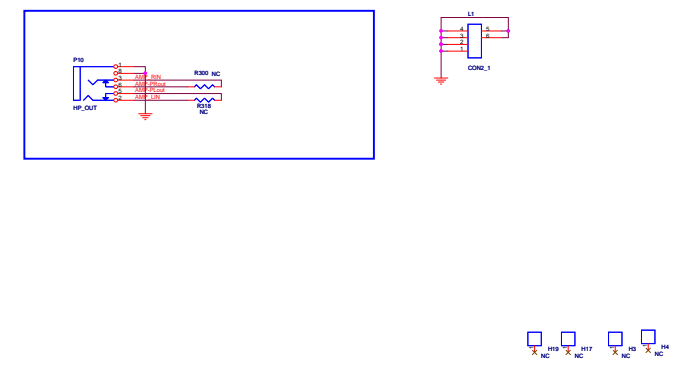
AUDIO pre-ap



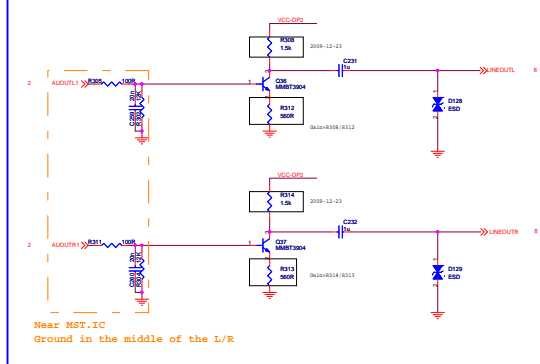
Power Down MUTE



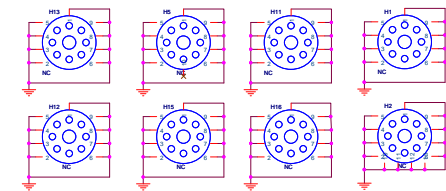
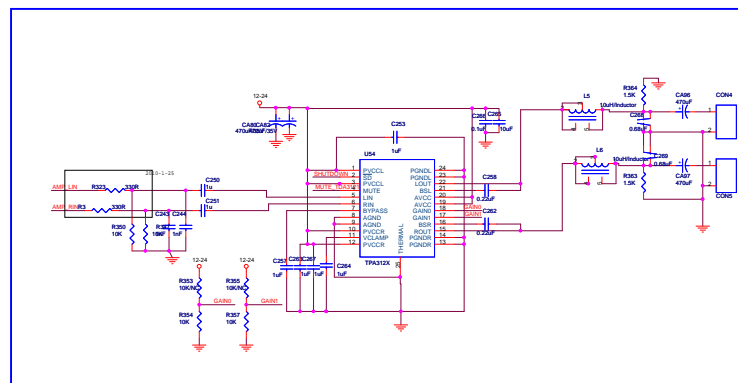
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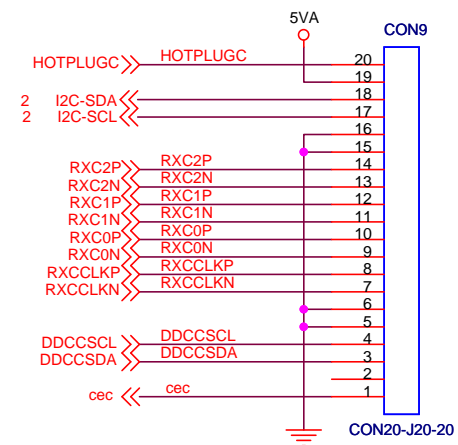
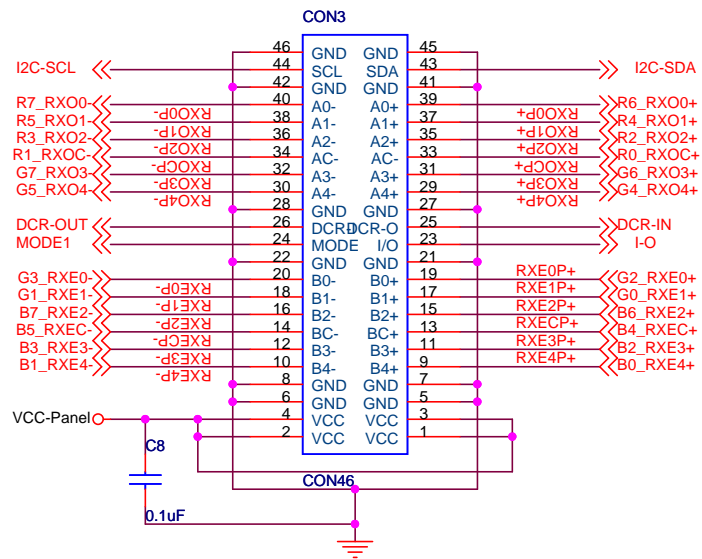


AUDIO pre-ap



TDA3121

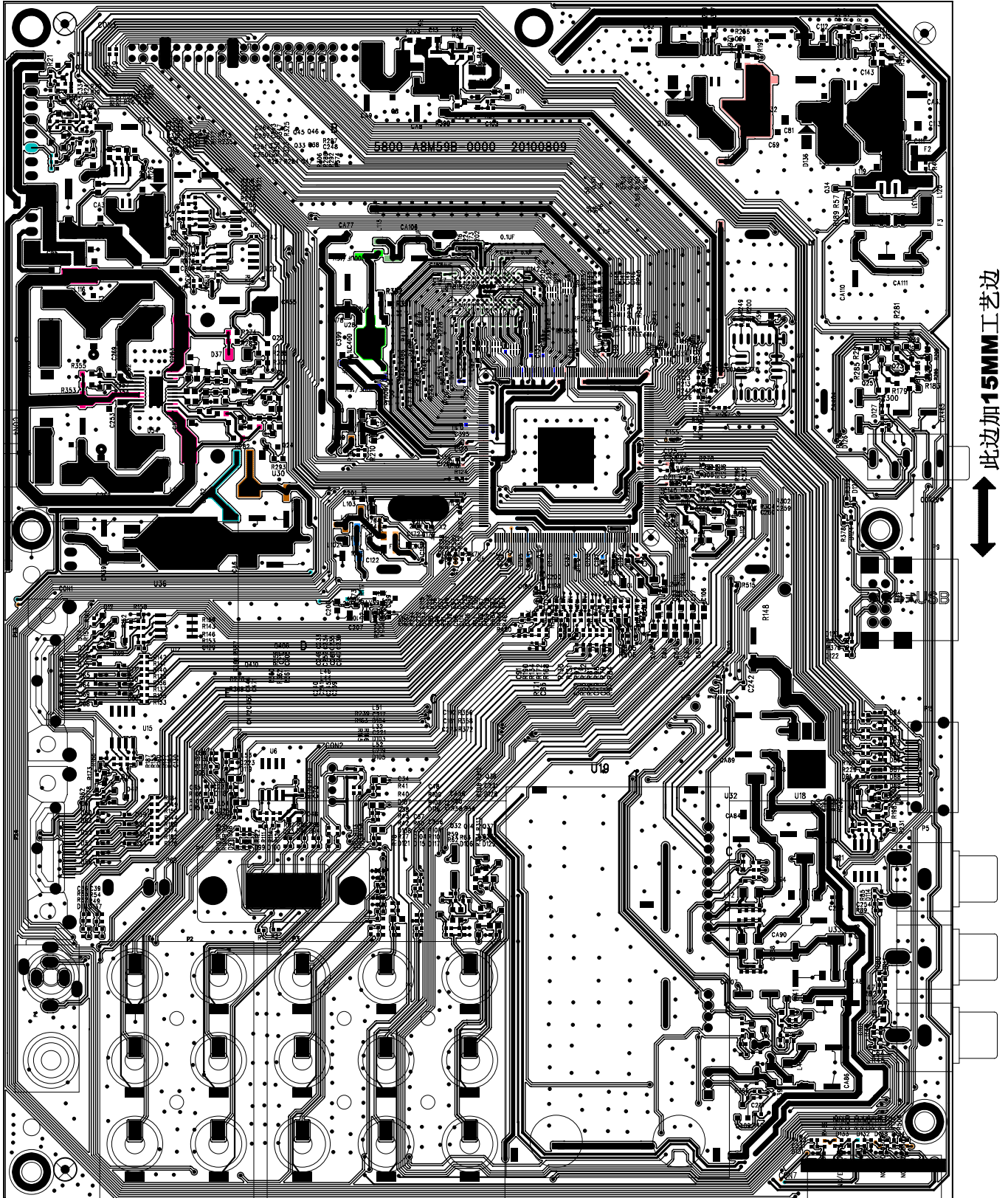




Title			
VIF 256p demo Board			
Size	Document Number		Rev
Custom	Panel Interface		1.0
Date:	Saturday, November 07, 2009	Sheet	11 of 12

此边加**5MM**工艺边

此边加**5MM**工艺边

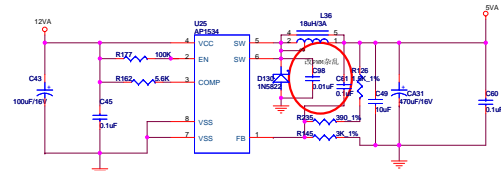


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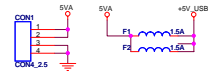


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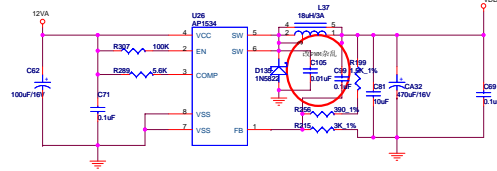
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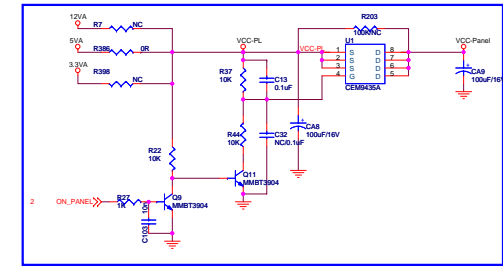
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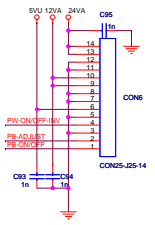
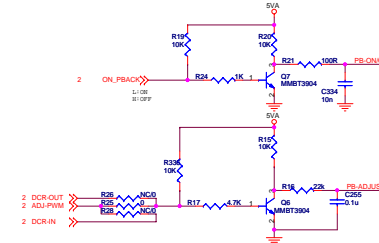
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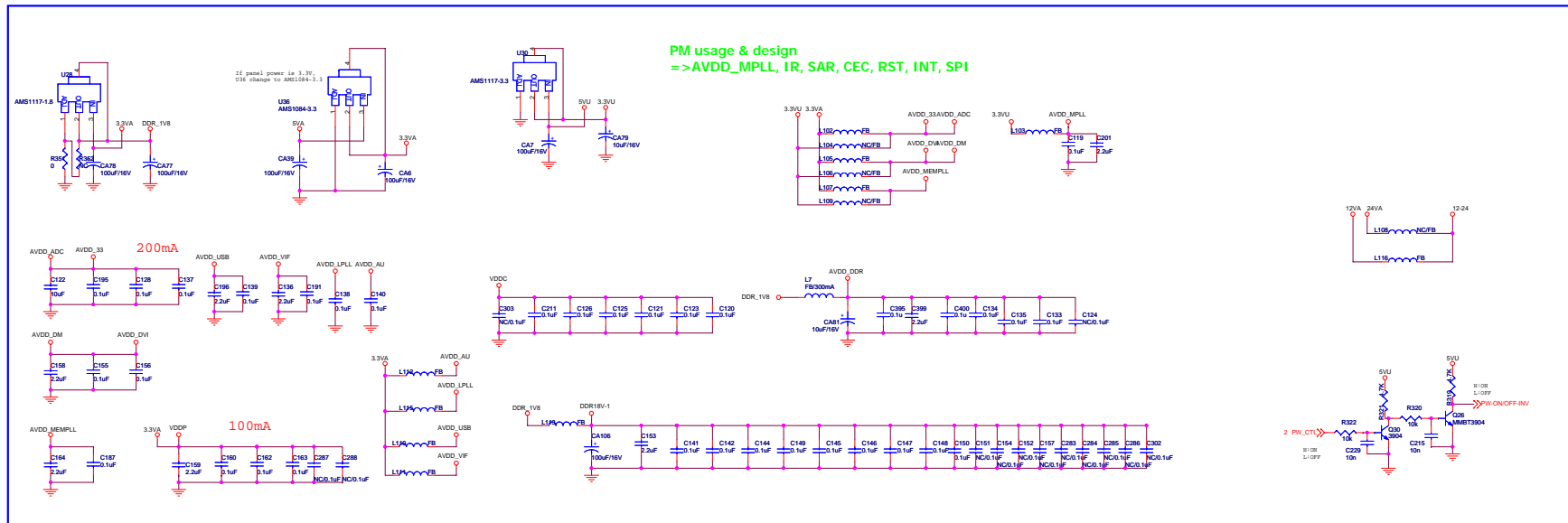
PANEL POWER



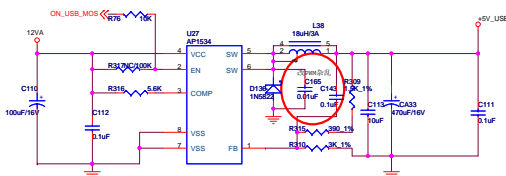
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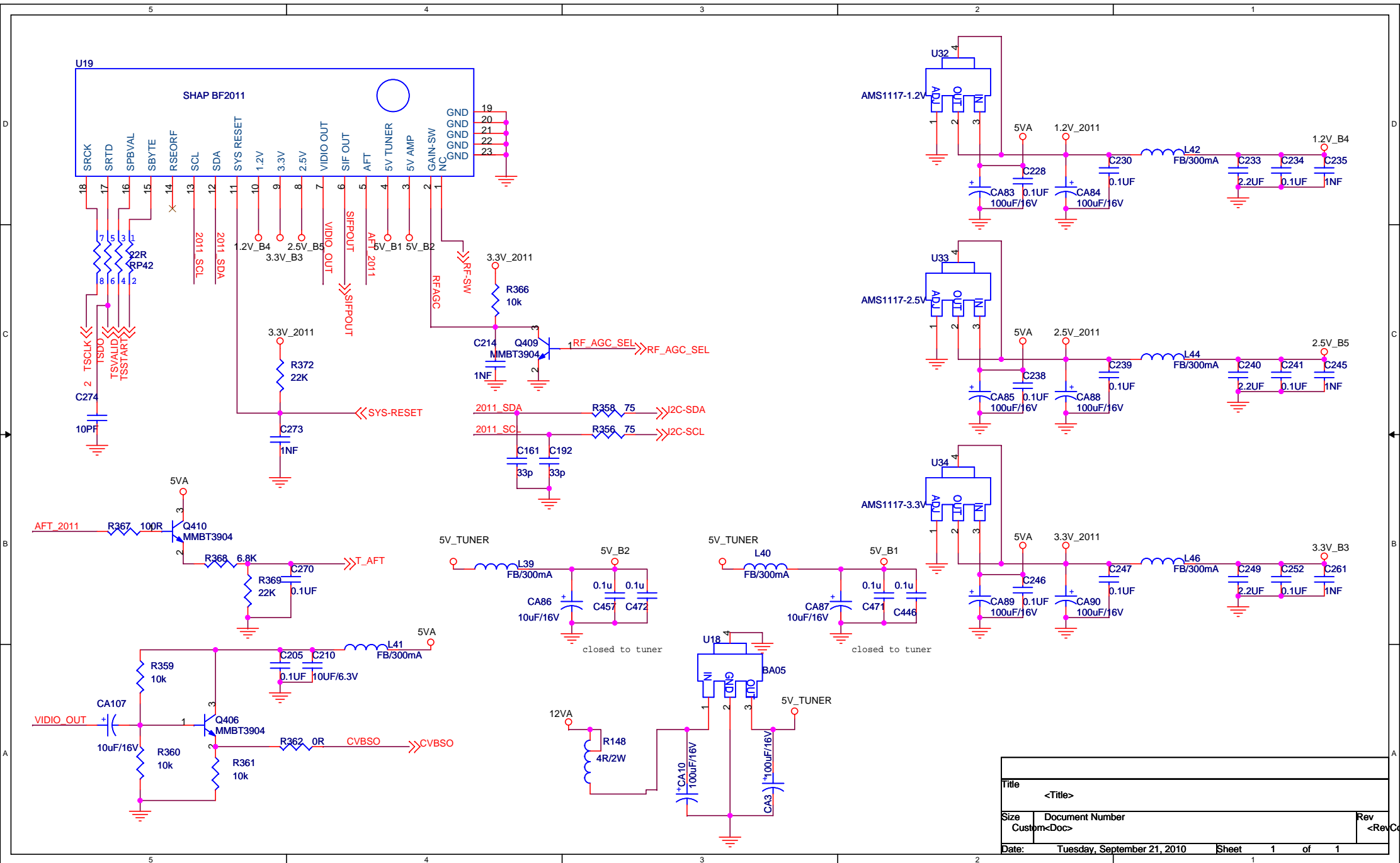
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USB Power

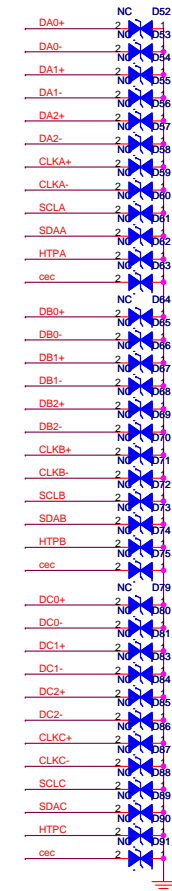
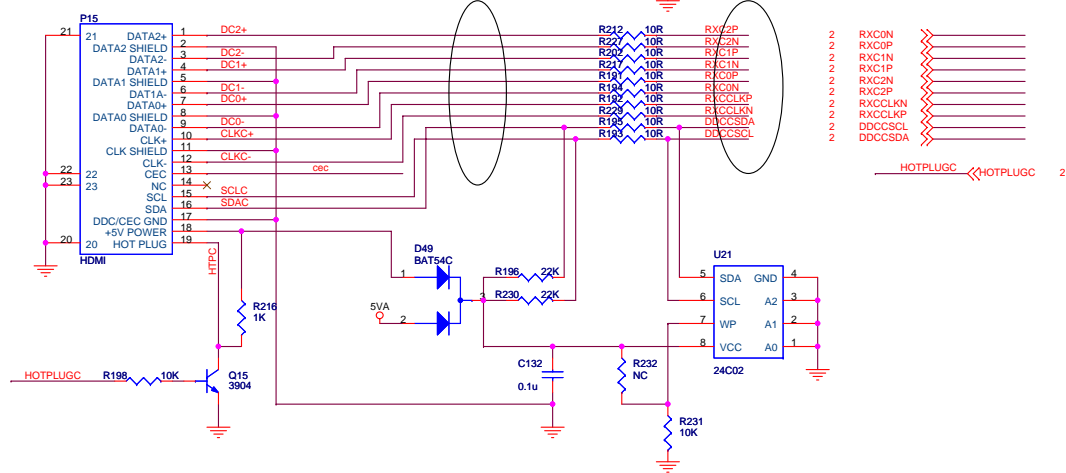
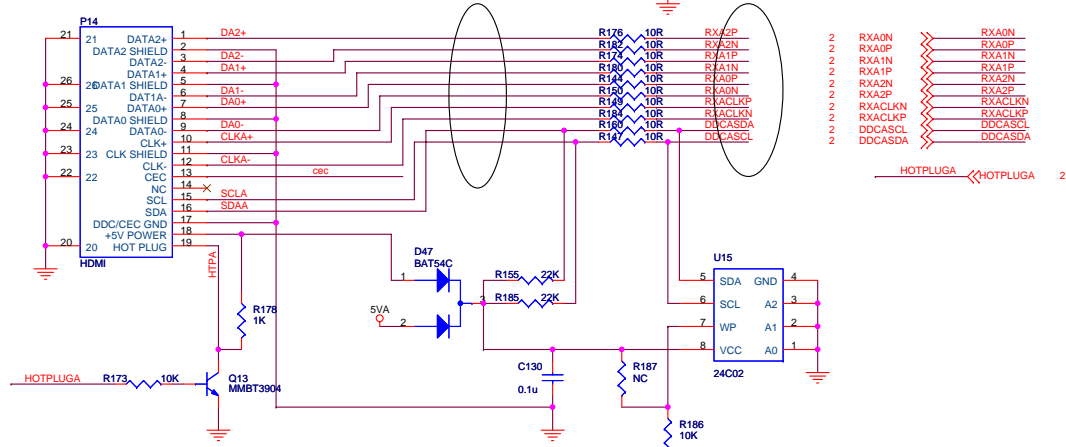
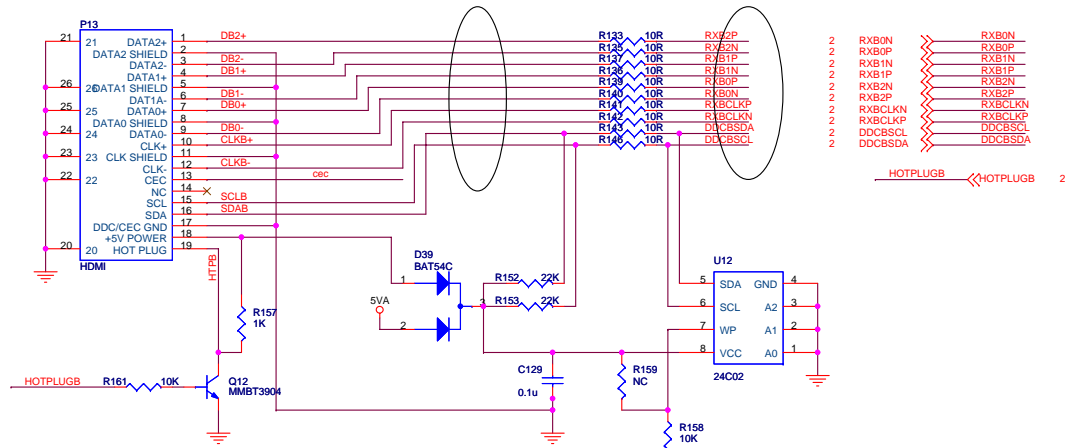


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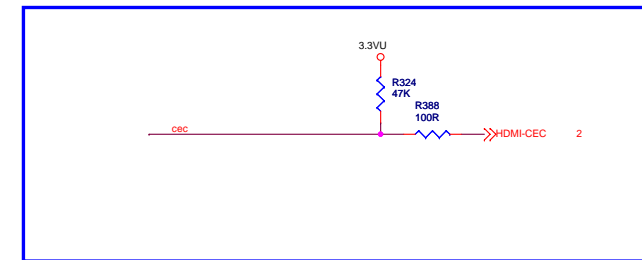


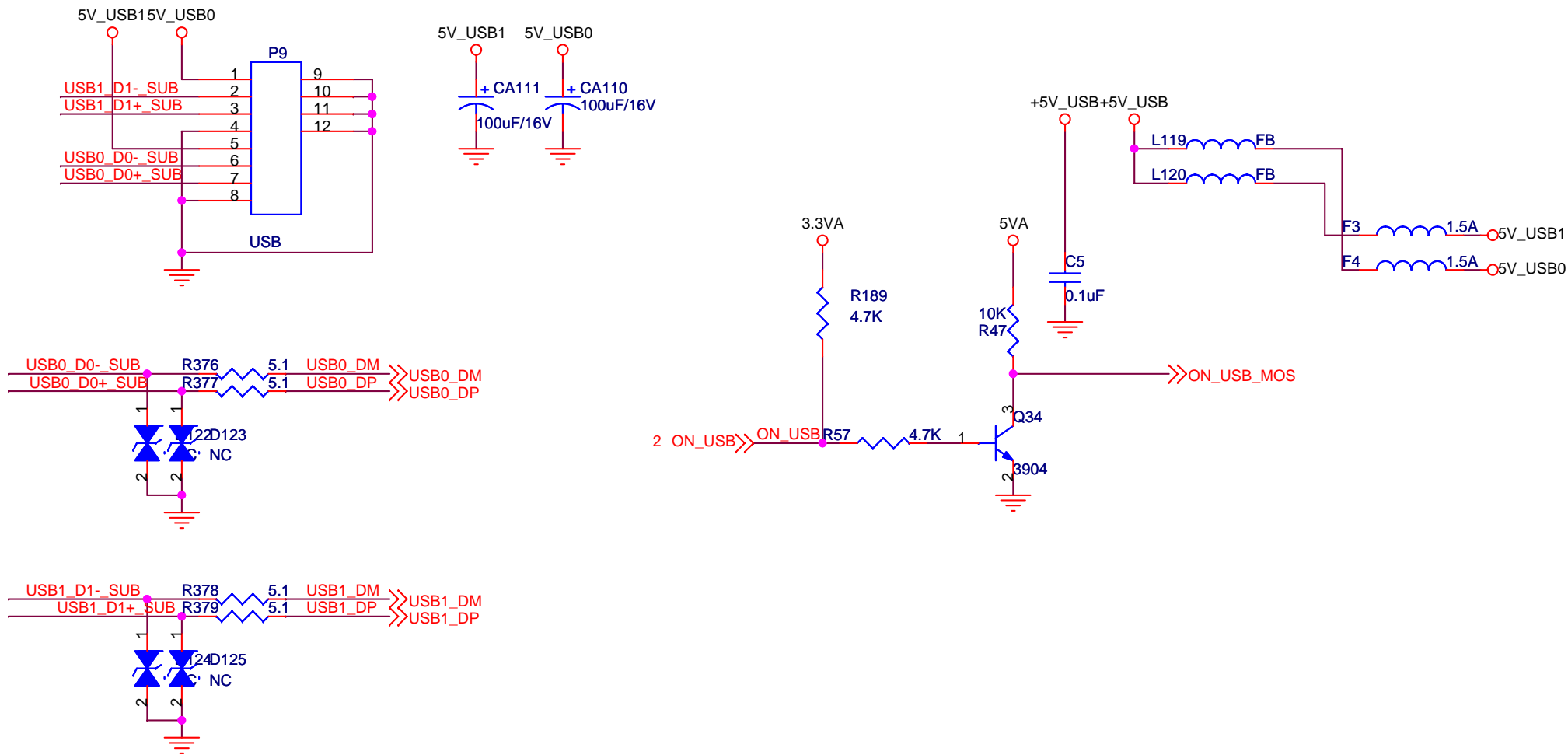
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Custom		<Doc>	<Rev Code>
Date:	Tuesday, September 21, 2010	Sheet	1 of 1

HDMI Input



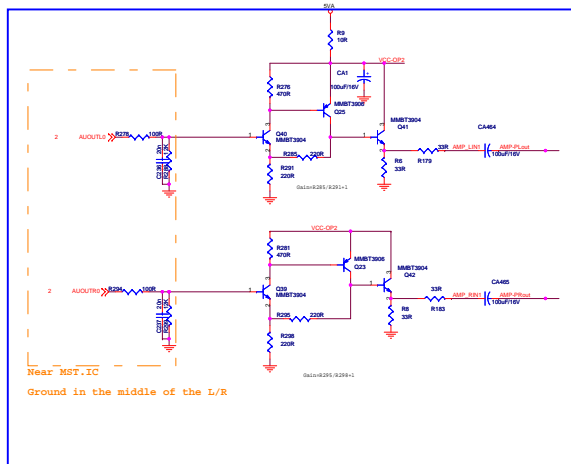
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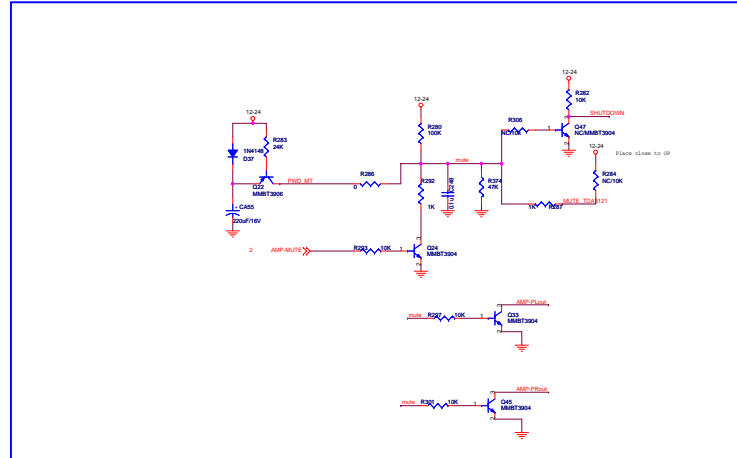


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VIF 256p demo Board			
Size	Document Number		Rev
Custom	USB		1.0
Date:	Tuesday, September 21, 2010	Sheet	8 of 12

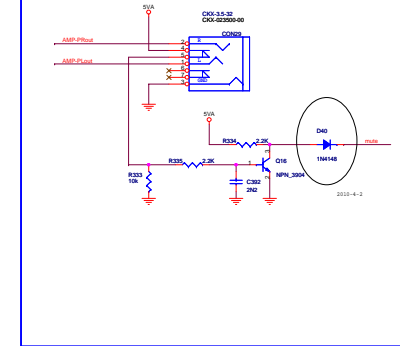
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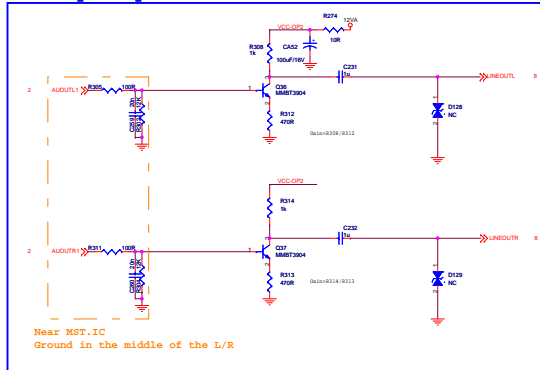
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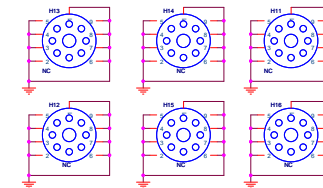
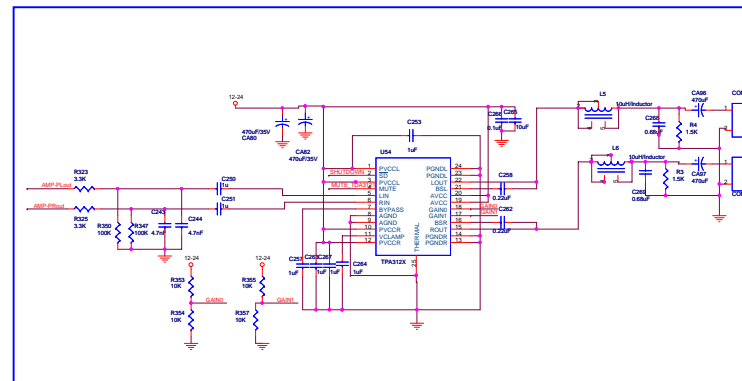
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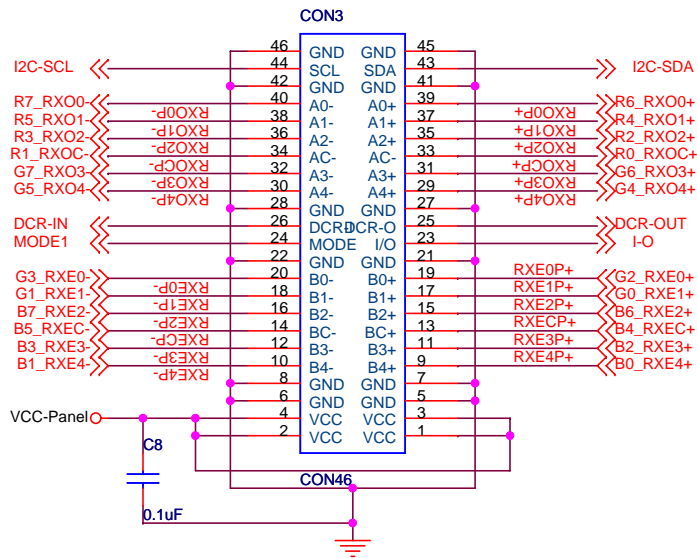


AUDIO pre-ap



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Title			
VIF 256p demo Board			
Size	Document Number		Rev
Custom	Panel Interface		1.0
Date:	Friday, September 25, 2009	Sheet	11 of 12

JSK4210-022B SPECIFICATION

Section 目录

1. Power supply overview 电源性能指标

1.1 Input Electrical Characteristics Overview (输入特性)

1.2 Output Electrical Characteristics Overview(输出特性)

1.2.1 Output Voltage, Current & Regulation.(输出电压电流调整率)

1.2.2 DC Output Ripple & Noise.(输出波纹和噪声)

1.3 On/Off Control:(ON/OFF控制)

1.4 Protection:(保护功能)

1.4.1 DC Output Over Voltage Protection .(输出过压保护)

1.4.2 DC Output Over Curent Protection.(输出过流保护)

1.4.3 DC Output Short Circuit Protection. (输出短流保护)

1.4.4 Reset After Shutoff.(保护功能复位)

2. Isolation 绝缘性能

3. Safety 安全规格

4. EMC 电磁兼容性

4.1 EMI (电磁干扰)

4.2 EMS (电磁抗扰)

5. Environmental Requirement 环境

5.1 Temperature (环境温度)

5.2 Humidity (环境湿度)

5.3 Altitude (海拔高度)

5.4 Cooling Method (冷却方式)

5.5 Vibration (振动耐受)

5.6 Impact (冲击耐受)


6. Dimension (物理尺寸)

7. Weight (重量)

8. Pin Connection (连接器脚位定义)

9. Power Supply mounting (安装尺寸)

10. Package、Transport、Storage(包装、运输、贮存)

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DATE	PREPARED	CHECKED	APPROVED	Document No.JSD20070601	REV:

1. Power Supply Overview 电性能指标:

1.1 Table 1 Input Electrical Characteristics Overview (输入特性)

Input voltage range 输入电压	90Vac-264Vac
Normal voltage range 标准输入	100Vac-240Vac
Frequency range 频率范围	50Hz/60Hz
Max input AC current 满载输入电流	90Vac/3A Max
Inrush current (cold start) 浪涌电流(冷机)	50A/100Vac; 100A/240Vac
Efficiency (full load) 效率	80% Min@115Vac,Full load
Harmonic current 谐波电流	GB17625.0-1998/IEC61000-3-2 CALSS D
Leakage Current 泄漏电流	≤0.75mA/220Vac
Standby Power Loss 待机功耗	≤1.0W/220Vac
Input Fuse 输入保险额定值	T5AL/250Vac

1.2 Output Eletrical Characteristics Overview (输出特性)

1.2.1 Table 2 Output Voltage, Current & Regulation. (输出调整率)

Output Voltage 输出电压	Regulation 调整率	Min current 最小电流	Rated current 额定电流
5VSB	±5%	0.1A	1A
5V	±5%	0.2A	2A
24V	±5%	0.2A	5A
12V	±5%	0.1A	2A

1.2.2 Table 3 DC Output Ripple & Noise. (输出波纹和噪声)


Output Voltage	Ripple & Noise(Max)
5VSB	Ripple≤80mV Noise≤150mV
5V	Ripple≤80mV Noise≤150mV
24V	Ripple≤240mV Noise≤500mV
12V	Ripple≤120mV Noise≤240mV

Note: 1)Measurements shall be made with an oscilloscopewith 20Mhz bandwidth .

示波器设置在20MHz带宽

2) Output shall be bypassed at the connector with a 0.1 uF ceramic capacitor and a 10uF electrolytic simulate system loading .

输出并联0.1uF的陶瓷电容和10uF的电解电容。

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DATE	PREPARED	CHECKED	APPROVED	Document No.JSD20070601	REV:

1.3 On/Off Control (ON/OFF控制)

The power supply DC outputs (without+5.0VSB) shall be enable with a high-level which more than 2.5V.
ON/OFF电平超过2.5V时, 电源输出正常。

The+5.0 VSB is on whenever the AC power is present.

只要AC输入, +5VSB就正常输出。

Table 1.

Ps-on Signal	Comments	Outputs
High	$\geq 2.5V$	Enable
Low	$\leq 1.5V$	Unable
Open		Unable

1.4 Protection:(保护功能)

1.4.1 Table9 DC Over Voltage Protection.(输出过压保护)

Output Voltage	Max. Over Voltage	Comments
24V	30V	Shut off
12V	16V	Shut off


1.4.2 Table 10 DC Output Over current Protection.(输出过流保护)

Output Voltage	Over Current	Comments
5VSB	3-11A	Hiccup
5V	3-11A	Hiccup
24V	8-15A	Shut off
12V	4-9A	Shut off

注:测5VSB之OCP时5V输出须空载, 同样测5V之OCP时5VSB输出须空载。

1.4.3 Table 11 DC Output Short Circuit Protection.(输出短路保护)

Output Voltage	Comments
5VSB	Hiccup
5V	Hiccup
24V	Shut off
12V	Shut off

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DATE	PREPARED	CHECKED	APPROVED	Document No.JSD20070601	REV:

1.4.4 Reset After Shutdown.(保护功能复位)

After power supply enter into shutdown,The power supply will rework after AC reset.

电源进入保护状态后，AC重置后电源才能重新正常工作。

2. Isolation (绝缘性能)

2.1 Table 12 (绝缘性能)

Input To Output	DC500V 4M Min (room temperature)

Note:

2.2 Table 13 (绝缘耐压)

Input To Output	3.0KV/10mA 50Hz 1 minute

Note:

3. Safety (安全规格)

The power supply shall compliance with the following Criterion:

电源安全性满足下列标准

1) GB8898-2001

4. EMC (电磁兼容性)

4.1 EMI (电磁干扰)

The power supply shall compliance with the following Criterion:

电源电磁干扰满足下列规则:

1) Conduction Emission:(传导干扰度)

EN55022, CLASS B

GB9254,CLASS B


* FCC PART15 CLASS B

2) Radiate Emission:(辐射干扰度)

EN55022, CLASS B

GB9254, CLASS B

* FCC PART15 CLASS B

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DATE	PREPARED	CHECKED	APPROVED	Document No.JSD20070601	REV:

4.2 EMS（电磁干扰）

The power supply shall compliance with the following Criterion:

电源电磁抗干扰满足下列规则：

1) ESD（静电抗扰度）

*GB17626.2-1998/IEC61000-4-2

2) EFT（脉冲群抗扰度）

*GB17626.4-1998/IEC61000-4-4 3KV

3) Surge（雷击浪涌）

*GB17626.5-1998/IEC61000-4-5 2KV/4KV

5. Environmental Requirement（工作环境）

5.1 Temperature（环境温度）

Operating : 0 °C to +40 °C

Store: -10 °C to +70 °C

5.2 Humidity（环境湿度）

Operating : From10% to 90% relative humidity (non-condensing).

Store: From 5 to 95% relative humidity (non-condensing).

5.3 Altitude（海拔高度）

Operating: To10, 000ft.

Store: To20, 000ft.

5.4 Cooling Method（冷却方式）

Ventilation cooling .

5.5 Vibration（振动耐受）

* 10-55Hz,49.0m/s²(5G),3minutes period, 60minutes each along X, Y and Z axis.

5.6 Impact（冲击耐受）

*196.1m/s²(20G), 11MS, once each X , Y and Z axis.


6.Dimension(物理尺寸)

*210mm x * 130mm x * 30 mm

7.Weight（重量）

*About 540g

备注:带“*”的为参考项.

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DATE	PREPARED	CHECKED	APPROVED	Document No. JSD20070601	REV:

8.Pin Connection (连接器脚位定义)

Table 14 CON1 Connection And Function

No.	Pin Connection	Function
1	L	AC INPUT L
2	N	AC INPUT N

Note: CON1 Pitch 3.96mm (三PIN中空,针脚180°直脚)

Table 15 CON2 CON5 Connection And Function

No.	Pin Connection	Function
1	GND	GND
2	GND	GND
3	GND	GND
4	GND	GND
5	GND	GND
6	24V	24V
7	24V	24V
8	24V	24V
9	24V	24V
10	24V	24V

Note: CON2 CON5 Pitch 2.5mm (针脚180°直脚)

Table 16 CON3 Connection And Function

No.	Pin Connection	Function
1	GND	GND
2	12V	12V
3	GND	GND
4	12V	12V

Note: CON3 Pitch:2.5mm (针脚180°直脚)



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				Model No.:	
				JSK4210-022	
DATE	PREPARED	CHECKED	APPROVED	Document No.JSD20070601	REV:

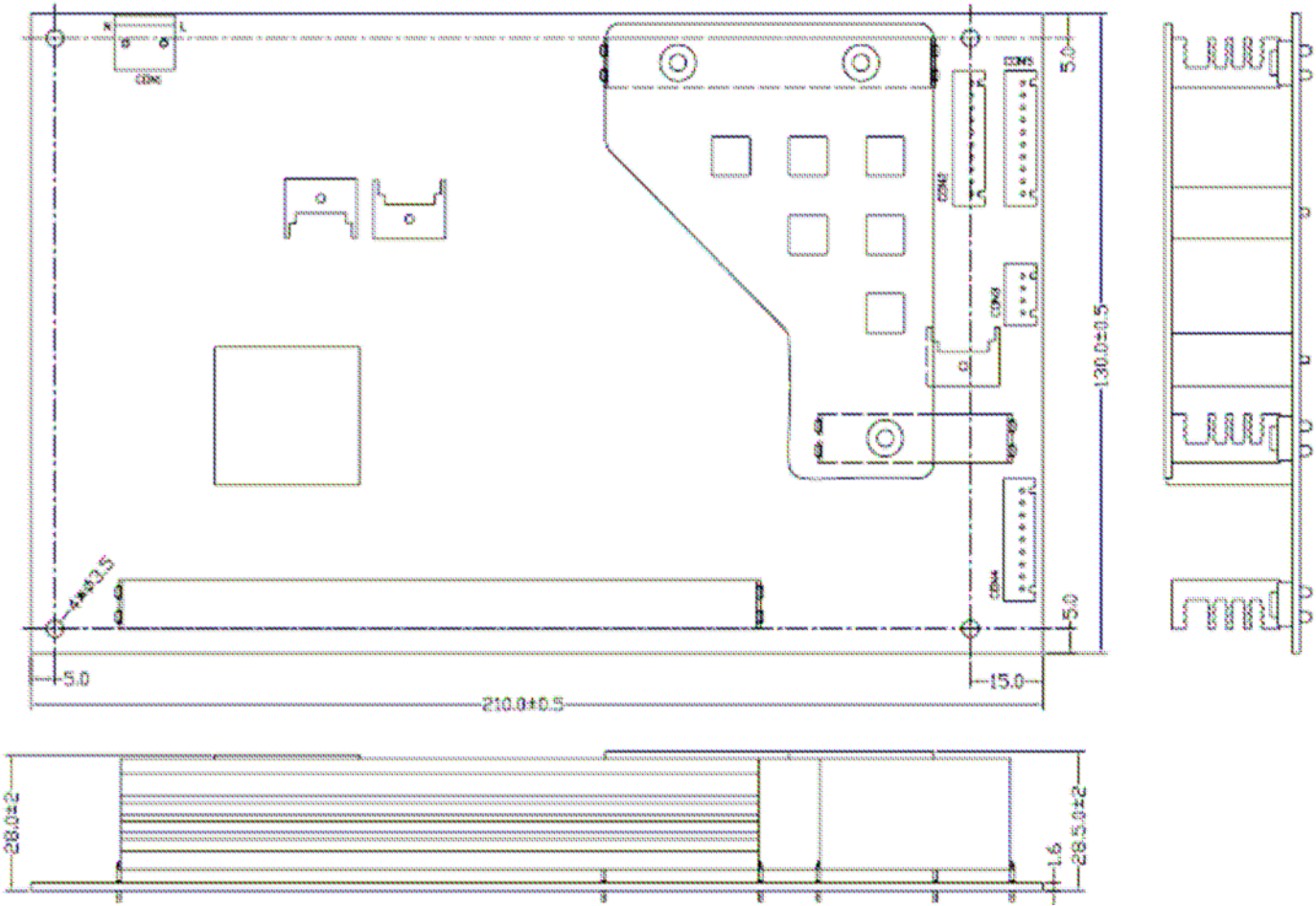
Table 17 CON4 Connection And Function


No	Pin Connection	Function
1	GND	GND
2	GND	GND
3	GND	GND
4	5V	5V
5	5V	5V
6	5V	5V
7	GND	GND
8	5VSB	5VSB
9	PS-ON	PS-ON

Note: CON4 Pitch:2.5mm (针脚180°直脚)

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DATE	PREPARED	CHECKED	APPROVED	Document No.JSD20070601	REV:

9. Power Supply mounting (安装尺寸)



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DATE	PREPARED	CHECKED	APPROVED	Document No.JSD20070601	REV:

10. Packing,Shipping and Storing (包装、运输、贮存)

1、Packing(包装)

Product name, part number, supplier's logo, QC stamp, Pb-free display and date must be printed on the package case.
包装箱上有产品名称、型号、厂家标识、厂家质量部门的检验合格证、制造日期等。


2、Shipping(运输)

This product can be transported through land, sea or air. Measures should be taken for water and sunproof.
Also, it should be handled with care
适应于车、船、飞机运输，运输中应遮蓬、防晒、文明装卸。

3、Storing(贮存)

Keep the product staying in the package case before using. The temperature of the stock house should be between -40-+55 C and the humidity should between 5-95%. Keep the product away from hazardous gas, flammable or explosive substances and erosive chemical material. Avoid dramatic vibration or shock and strong magnetic field. The package cases should be racked 20cm above the ground and 50cm away from the wall, window,heat source or ventilation port. Generally the storage term of this product is 2 years. All the products should be doublechecked after that time.

产品未使用时应存放在包装箱内，仓库环境温度为-40℃—55℃，相对湿度为5%—95%，仓库内不允许有有害气体，易燃，易爆的产品及有腐蚀性的化学物品，并且无强烈的机械振动，冲击和强磁场作用，包装箱应垫离地至少20cm高，距离墙壁、热源、窗口或空气入口至少50cm，在本规定条件下的贮存期一般为2年，超过2年后应重新进行检验。

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DATE	PREPARED	CHECKED	APPROVED	Document No.JSD20070601	REV:

JSK4210-022B SCHEMATIC

JSK4210-022B IC DATASHEETS

IC Characteristic for LCD TV Power Supply

PWM IC(IC6) : L6599



L6599

HIGH-VOLTAGE RESONANT CONTROLLER

TARGET SPEC

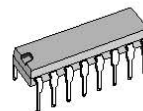
MAIN FEATURES

- 50% DUTY CYCLE, VARIABLE FREQUENCY CONTROL OF RESONANT HALF-BRIDGE
- HIGH-ACCURACY OSCILLATOR
- UP TO 500 kHz OPERATING FREQUENCY
- TWO-LEVEL OCP: FREQUENCY-SHIFT AND LATCHED SHUTDOWN
- INTERFACE WITH PFC CONTROLLER
- LATCHED DISABLE INPUT
- BURST-MODE OPERATION AT LIGHT LOAD
- INPUT FOR POWER-ON/OFF SEQUENCING OR BROWNOUT PROTECTION
- NON-LINEAR SOFT-START FOR MONOTONIC OUTPUT VOLTAGE RISE
- 600V-RAIL COMPATIBLE HIGH-SIDE GATE DRIVER WITH INTEGRATED BOOTSTRAP DIODE AND HIGH dV/dt IMMUNITY
- -300/800 mA HIGH-SIDE AND LOW-SIDE GATE DRIVERS WITH UVLO PULL-DOWN
- DIP16, SO16N PACKAGE

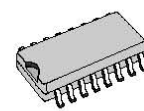
APPLICATIONS

- LCD & PDP TV
- DESKTOP PC, ENTRY-LEVEL SERVER
- TELECOM SMPS
- AC-DC ADAPTER, OPEN FRAME SMPS

BCD OFFLINE TECHNOLOGY



DIP16



SO16N

ORDERING NUMBERS:

L6599N

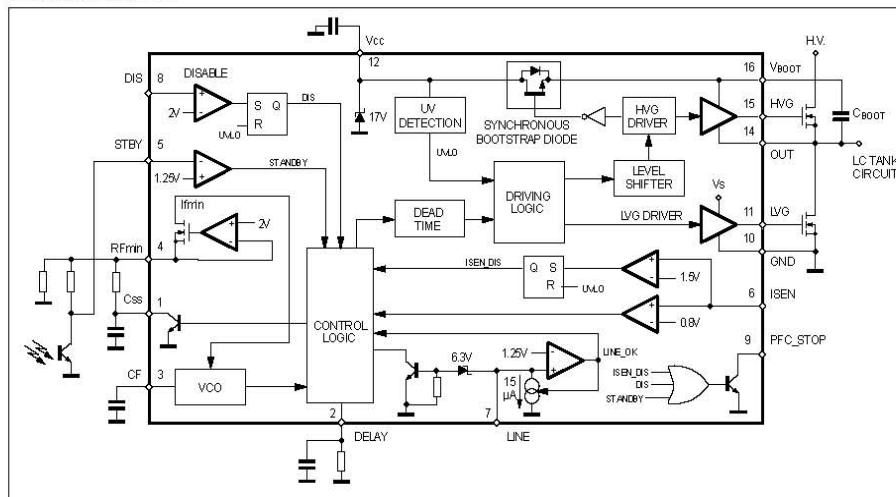
L6599D

L6599TR

DESCRIPTION

The L6599 is a double-ended controller specific for the series-resonant half-bridge topology. It provides 50% complementary duty cycle: the high-side switch and the low-side switch are driven ON 180° out-of-phase for exactly the same time. Output voltage regulation is obtained by modulating the operating frequency. A fixed dead-time inserted between the turn-off of one switch

BLOCK DIAGRAM



April 2005

1/17

This is preliminary information on a new product foreseen to be developed. Details are subject to change without notice.

L6599

and the turn-on of the other one guarantees soft-switching and enables high-frequency operation.

To drive the high-side switch with the bootstrap approach, the IC incorporates a high-voltage floating structure able to withstand more than 600V with a synchronous-driven high-voltage DMOS that replaces the external fast-recovery bootstrap diode.

The IC enables the designer to set the operating frequency range of the converter by means of an externally programmable oscillator.

At start-up, to prevent uncontrolled inrush current, the switching frequency starts from a programmable maximum value and progressively decays until it reaches the steady-state value determined by the control loop. This frequency shift is non linear to minimize output voltage overshoots; its duration is programmable as well.

At light load the IC enters a controlled burst-mode operation that keeps the converter input consumption to a minimum.

IC's functions include a not-latched active-low disable input with current hysteresis useful for power sequencing or for brownout protection, a current sense input for OCP with frequency shift and delayed shutdown with automatic restart. A higher level OCP latches off the IC if the first-level protection is not sufficient to control the primary current. Their combination offers complete protection against overload and short circuits. An additional latched disable input (DIS) allows easy implementation of OTP and/or OVP.

An interface with the PFC controller is provided that enables to switch off the pre-regulator during fault conditions, such as OCP shutdown and DIS high, or during burst-mode operation.

ABSOLUTE MAXIMUM RATINGS

Symbol	Pin	Parameter	Value	Unit
V _{BOOT}	16	Floating supply voltage	-1 to 618	V
V _{OUT}	14	Floating ground voltage	-3 to V _{BOOT} -18	V
dV _{OUT} /dt	14	Floating ground max. slew rate	50	V/ns
V _{CC}	12	IC Supply voltage (I _{CC} ≤ 25 mA)	Self-limited	V
V _{PFC_STOP}	9	Maximum voltage (pin open)	-0.3 to V _{CC}	V
I _{PFC_STOP}	9	Maximum sink current (pin low)	Self-limited	A
V _{LINEmax}	7	Maximum pin voltage (I _{pin} ≤ 1mA)	Self-limited	V
I _{RFmin}	4	Maximum source current	2	mA
---	1 to 6, 8	Analog Inputs & Outputs	-0.3 to 5	V
f _{oscmax}		Maximum operating frequency	500	kHz
P _{tot}		Power Dissipation @T _{amb} = 70°C (DIP16)	1	W
		Power Dissipation @T _{amb} = 50°C (SO16)	0.83	
T _j		Junction Temperature Operating range	-40 to 150	°C
T _{stg}		Storage Temperature	-55 to 150	°C

Note: ESD immunity for pins 14, 15 and 16 is guaranteed up to 900V (Human Body Model)

PIN CONNECTION (Top view)

Css	1	16	VBOOT
DELAY	2	15	HVG
CF	3	14	OUT
RFmin	4	13	N.C.
STBY	5	12	Vcc
ISEN	6	11	LVG
LINE	7	10	GND
DIS	8	9	PFC_STOP

THERMAL DATA

Symbol	Parameter	Value	Unit
R _{th j-amb}	Max. Thermal Resistance, Junction-to-ambient (DIP16)	80	°C/W
	Max. Thermal Resistance, Junction-to-ambient (SO16)	120	



L6599

PIN FUNCTIONS

N.	Name	Function
1	Css	Soft start. This pin connects an external capacitor to GND and a resistor to RFmin (pin 4) that set both the maximum oscillator frequency and the time constant for the frequency shift that occurs as the chip starts up (soft-start). An internal switch discharges this capacitor every time the chip turns off ($V_{CC} < UVLO$, $LINE < 1.25\text{ V}$ or $> 6\text{ V}$, $DIS > 2\text{ V}$, $ISEN > 1.5\text{ V}$, $DELAY > 2\text{ V}$) to make sure it will be soft-started next, and when the voltage on the current sense pin (ISEN) exceeds 0.8 V , as long as it stays above 0.75 V .
2	DELAY	Delayed shutdown upon overcurrent. A capacitor and a resistor are connected from this pin to GND to set the maximum duration of an overcurrent condition before the IC stops switching and the delay after which the IC restarts switching. Every time the voltage on the ISEN pin exceeds 0.8 V the capacitor is charged by an internal $150\text{ }\mu\text{A}$ current generator and is slowly discharged by the external resistor. If the voltage on the pin reaches 2 V , the soft start capacitor is completely discharged so that the switching frequency is pushed to its maximum value and the $150\text{ }\mu\text{A}$ is kept always on. As the voltage on the pin exceeds 3.5 V the IC stops switching and the internal generator is turned off, so that the voltage on the pin will decay because of the external resistor. The IC will be soft-restarted as the voltage drops below 0.3 V . In this way, under short circuit conditions, the converter will work intermittently with very low input average power.
3	CF	Timing capacitor. A capacitor connected from this pin to GND is charged and discharged by internal current generators programmed by the external network connected to pin 4 (RFmin) and determines the switching frequency of the converter.
4	RFmin	Minimum oscillator frequency setting. This pin provides a precise 2 V reference and a resistor connected from this pin to GND defines a current that is used to set the minimum oscillator frequency. To close the feedback loop that regulates the converter output voltage by modulating the oscillator frequency, the phototransistor of an optocoupler will be connected to this pin through a resistor. The value of this resistor will set the maximum operating frequency. An R-C series connected from this pin to GND sets frequency shift at start-up to prevent excessive energy inrush (soft-start).
5	STBY	Burst-mode operation threshold. The pin senses some voltage related to the feedback control, which is compared to an internal reference (1.25 V). If the voltage on the pin is lower than the reference, the IC enters an idle state and its quiescent current is reduced. The chip restarts switching as the voltage exceeds the reference by 50 mV . Soft-start is not invoked. This function realizes burst-mode operation when the load falls below a level that can be programmed by properly choosing the resistor connecting the optocoupler to pin RFmin (see block diagram). Tie the pin to RFmin if burst-mode is not used.
6	ISEN	Current sense input. The pin senses the primary current through a sense resistor or a capacitive divider for lossless sensing. This input is not intended for a cycle-by-cycle control; hence the voltage signal must be filtered to get average current information. As the voltage exceeds a 0.8 V threshold (with 50 mV hysteresis), the soft-start capacitor connected to pin 1 is internally discharged: the frequency increases hence limiting the power throughput. Under output short circuit, this normally results in a nearly constant peak primary current. This condition is allowed for a maximum time set at pin 2. If the current keeps on building up despite this frequency increase, a second comparator referenced at 1.5 V latches the device off and brings its consumption almost to a "before start-up" level. The information is latched and it is necessary to recycle the supply voltage of the IC to enable it to restart: the latch is removed as the voltage on the Vcc pin goes below the UVLO threshold. Tie the pin to GND if the function is not used.
7	LINE	Line sensing input. The pin is to be connected to the high-voltage input bus with a resistor divider to perform either AC or DC (in systems with PFC) brownout protection. A voltage below 1.25 V shuts down (not latched) the IC, lowers its consumption and discharges the soft-start capacitor. IC's operation is re-enabled (soft-started) as the voltage exceeds 1.25 V . The comparator is provided with current hysteresis: an internal $15\text{ }\mu\text{A}$ current generator is ON as long as the voltage applied at the pin is below 1.25 V and is OFF if this value is exceeded. Bypass the pin with a capacitor to GND to reduce noise pick-up. The voltage on the pin is top-limited by an internal zener. Activating the zener causes the IC to shut down (not latched). Tie the pin to RFmin if the function is not used.
8	DIS	Latched device shutdown. Internally the pin connects a comparator that, when the voltage on the pin exceeds 2 V , shuts the IC down and brings its consumption almost to a "before start-up" level. The information is latched and it is necessary to recycle the supply voltage of the IC to enable it to restart: the latch is removed as the voltage on the Vcc pin goes below the UVLO threshold. Tie the pin to GND if the function is not used.

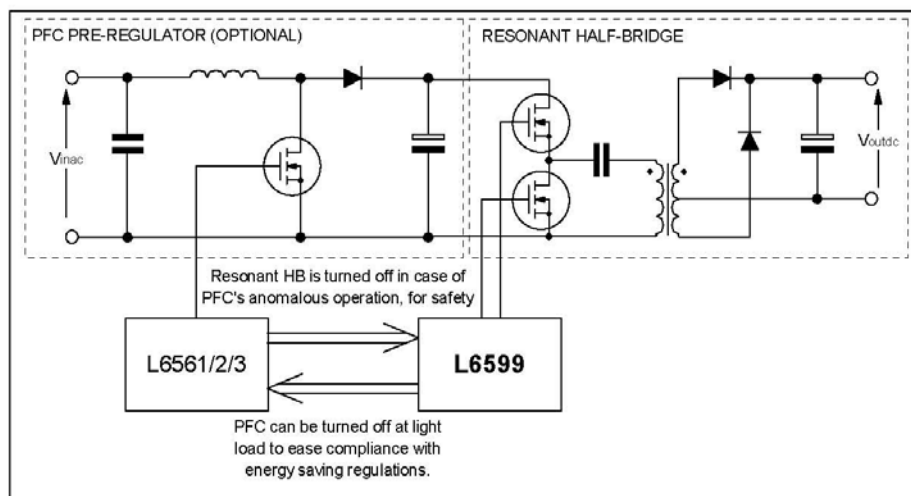


L6599

PIN FUNCTIONS (cont'd)

9	PFC_STOP	Open-drain ON/OFF control of PFC controller. This pin, normally open, is intended for stopping the PFC controller, for protection purpose or during burst-mode operation. It goes low when the IC is shut down by DIS>2 V, ISEN>1.5 V, LINE>6 V and STBY<1.25V. The pin is pulled low also when the voltage on pin DELAY exceeds 2V and goes back open as the voltage falls below 0.3V. During UVLO, it is open. Leave the pin unconnected if not used.
10	GND	Chip ground. Current return for both the low-side gate-drive current and the bias current of the IC. All of the ground connections of the bias components should be tied to a track going to this pin and kept separate from any pulsed current return.
11	LVG	Low-side gate-drive output. The driver is capable of 0.3 A min. source and 0.8 A min. sink peak current to drive the lower MOSFET of the half-bridge leg. The pin is actively pulled to GND during UVLO.
12	Vcc	Supply Voltage of both the signal part of the IC and the low-side gate driver. Sometimes a small bypass capacitor (0.1 μ F typ.) to GND might be useful to get a clean bias voltage for the signal part of the IC.
13	N.C.	High-voltage spacer. The pin is not internally connected to isolate the high-voltage pin and ease compliance with safety regulations (creepage distance) on the PCB.
14	OUT	High-side gate-drive floating ground. Current return for the high-side gate-drive current. Layout carefully the connection of this pin to avoid too large spikes below ground.
15	HVG	High-side floating gate-drive output. The driver is capable of 0.3A min. source and 0.8A min. sink peak current to drive the upper MOSFET of the half-bridge leg. A resistor internally connected to pin 14 (OUT) ensures that the pin is not floating during UVLO.
16	VBOOT	High-side gate-drive floating supply Voltage. The bootstrap capacitor connected between this pin and pin 14 (OUT) is fed by an internal synchronous bootstrap diode driven in-phase with the low-side gate-drive. This patented structure replaces the normally used external diode.

TYPICAL SYSTEM BLOCK DIAGRAM



L6599

ELECTRICAL CHARACTERISTICS (Tj=0 to 105°C, Vcc=15V, VBOOT=15V, CHVG=CLVG=1 nF; CF=470 pF; RRFmin=12 kΩ; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
IC SUPPLY VOLTAGE						
Vcc	Operating range	After device turn-on	8.7		16	V
VccOn	Turn-on threshold	Voltage rising	10	10.7	11.4	V
VccOff	Turn-off threshold	Voltage falling	7.45	8.15	8.85	V
Hys	Hysteresis			2.55		V
Vz	Vcc clamp voltage	Iclamp = 10 mA	16	17	17.5	V
SUPPLY CURRENT						
Istart-up	Start-up Current	Before device turn-on Vcc = VccOn - 0.2 V		200	250	μA
Iq	Quiescent Current	Device on, VSTBY = 1V		1.5	2	mA
Iop	Operating current			4		mA
Iq	Residual consumption	VDIS > 2 V or VDELAY > 2V or VLINE < 1.25 V or VLINE = Vclamp		300	400	μA
HIGH-SIDE FLOATING GATE-DRIVE SUPPLY						
ILKBOOT	VBOOT pin leakage current	VBOOT = 580V			5	μA
ILKOUT	OUT pin leakage current	VOUT = 562V			5	μA
RDS(on)	Synchronous bootstrap diode on-resistance	VLVG = HIGH		150		Ω
OVERCURRENT COMPARATOR						
ISEN	Input Bias Current	VISEN = 0 to VISENdis			-1	μA
tLEB	Leading Edge Blanking	After VHVG and VLVG low-to-high transition		250		ns
VISENx	Frequency shift threshold	Voltage rising ⁽¹⁾	0.76	0.8	0.84	V
	Hysteresis	Voltage falling		50		mV
VISENdis	Latch off threshold	Voltage rising ⁽¹⁾	1.44	1.5	1.56	V
td(H-L)	Delay to Output				200	ns
LINE SENSING						
Vth	Threshold voltage	Voltage rising or falling ⁽¹⁾	1.2	1.25	1.3	V
IHys	Current Hysteresis	Vcc > 5V, VLINE = 0.3V	12	15	18	μA
Vclamp	Clamp level	ILINE = 1mA	6		8	V
DIS FUNCTION						
IDIS	Input Bias Current	VDIS = 0 to Vth			-1	μA
Vth	Disable threshold	Voltage rising ⁽¹⁾⁽²⁾	1.92	2	2.08	V
OSCILLATOR						
D	Output duty cycle	Both HVG and LVG	48	50	52	%
fosc	Oscillation frequency		58.2	60	61.8	kHz
		RRFmin = 3.48 kΩ	240	250	260	
TD	Dead-time	Between HVG and LVG	0.2	0.27	0.35	μs
VCFp	Peak value			3.9		V
VCFv	Valley value			0.8		V
VREF	Voltage reference at pin 4	⁽¹⁾	1.92	2	2.08	V
KM	Current mirroring ratio			1		A/A
PFC_STOP FUNCTION						
Ileak	High level leakage current	VPFC_STOP = Vcc, VDIS = 0 V			1	μA
VL	Low saturation level	IPFC_STOP = 1mA, VDIS = 1.5 V			0.1	V



5/17

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L6599

ELECTRICAL CHARACTERISTICS (cont'd)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SOFT-START FUNCTION						
I_{leak}	Open-state current	$V(Css) = 2V$			0.5	μA
R	Discharge resistance	$V_{ISEN} > V_{ISENx}$		100		Ω
STANDBY FUNCTION						
I_{DIS}	Input Bias Current	$V_{DIS} = 0$ to V_{th}			-1	μA
V_{th}	Disable threshold	Voltage falling ⁽¹⁾	1.2	1.25	1.3	V
Hys	Hysteresis	Voltage rising		50		mV
DELAYED SHUTDOWN FUNCTION						
I_{leak}	Open-state current	$V(DELAY) = 0$			0.5	μA
I_{CHARGE}	Charge current	$V_{DELAY} = 1V$, $V_{ISEN} = 0.85V$	100	150	200	μA
T_{CHARGE}	Charge duration			20		μs
V_{th1}	Threshold for forced operation at max. frequency	Voltage rising ⁽¹⁾	1.92	2	2.08	V
V_{th2}	Shutdown threshold	Voltage rising ⁽¹⁾	3.3	3.5	3.7	V
V_{th3}	Restart threshold	Voltage falling ⁽¹⁾	0.25	0.3	0.35	V
LOW-SIDE GATE DRIVER (voltages referred to GND)						
V_{LVGL}	Output Low Voltage	$I_{sink} = 200 mA$			1.5	V
V_{LVGH}	Output High voltage	$I_{source} = 5 mA$	12.8	13.3		V
$I_{sourcepk}$	Peak source current		-0.3			A
I_{sinkpk}	Peak sink current		0.8			A
t_f	Fall Time			30		ns
t_r	Rise Time			60		ns
	UVLO saturation	$V_{cc} = 0$ to $V_{cc_{On}}$, $I_{sink} = 2mA$			1.1	V
HIGH-SIDE GATE DRIVER (voltages referred to OUT)						
V_{LVGL}	Output Low Voltage	$I_{sink} = 200 mA$			1.5	V
V_{LVGH}	Output High voltage	$I_{source} = 5 mA$	12.8	13.3		V
$I_{sourcepk}$	Peak source current		-0.3			A
I_{sinkpk}	Peak sink current		0.8			A
t_f	Fall Time			30		ns
t_r	Rise Time			60		ns
	HVG-OUT pull-down			25		$k\Omega$

⁽¹⁾ Values tracking each other

⁽²⁾ This value will be reduced at 1.82V typ. in the final silicon release





April 2006

FAN7602

Green Current Mode PWM Controller

Features

- Green Current Mode PWM Control
- Fixed 65kHz Operation with Frequency Modulation
- Internal High-Voltage Start-up Switch
- Burst Mode Operation
- Line Voltage Feed Forward to Limit Maximum Power
- Line Under-Voltage Protection
- Latch Protection & Internal Soft-Start (10ms) Function
- Overload Protection
- Over Voltage Protection
- Low Operation Current: Typ. 1mA
- 8-pin DIP

Applications

- Adapter
- LCD Monitor Power
- Auxiliary Power Supply

Related Application Notes

- AN6014 - Green Current Mode PWM Controller FAN7602

Description

The FAN7602 is a green current mode PWM controller. It is specially designed for off-line adapter application, DVDP, VCR, LCD monitor application, and auxiliary power supplies.

The internal high-voltage start-up switch and the burst mode operation reduce the power loss in standby mode. Because of the internal start-up switch and the burst mode, it is possible to supply 0.5W load limiting the input power under 1W when the input line voltage is 265Vac. On no-load condition, the input power is under 0.3W.

The maximum power can be limited constantly, regardless of the line voltage change using the power limit function.

The switching frequency is internally fixed to be 65kHz and the frequency modulation technique reduces EMI.

The FAN7602 includes various protections for the system reliability and the internal soft start prevents the output voltage over-shoot at start-up.

Ordering Information

Part Number	Operating Temp. Range	Pb-Free	Package	Packing Method	Marking Code
FAN7602N	-25°C to +125°C	Yes	8-DIP	Rail	FAN7602

Typical Application Diagram

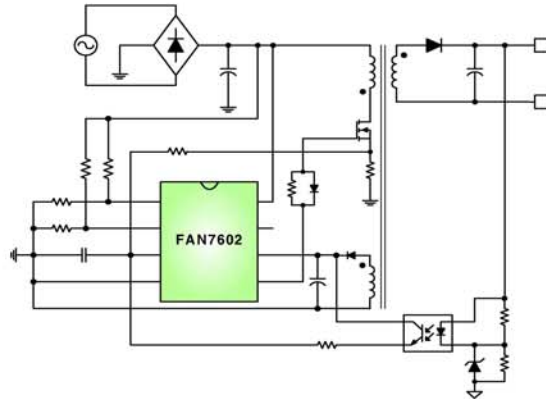


Figure 1. Typical Flyback Application

Internal Block Diagram

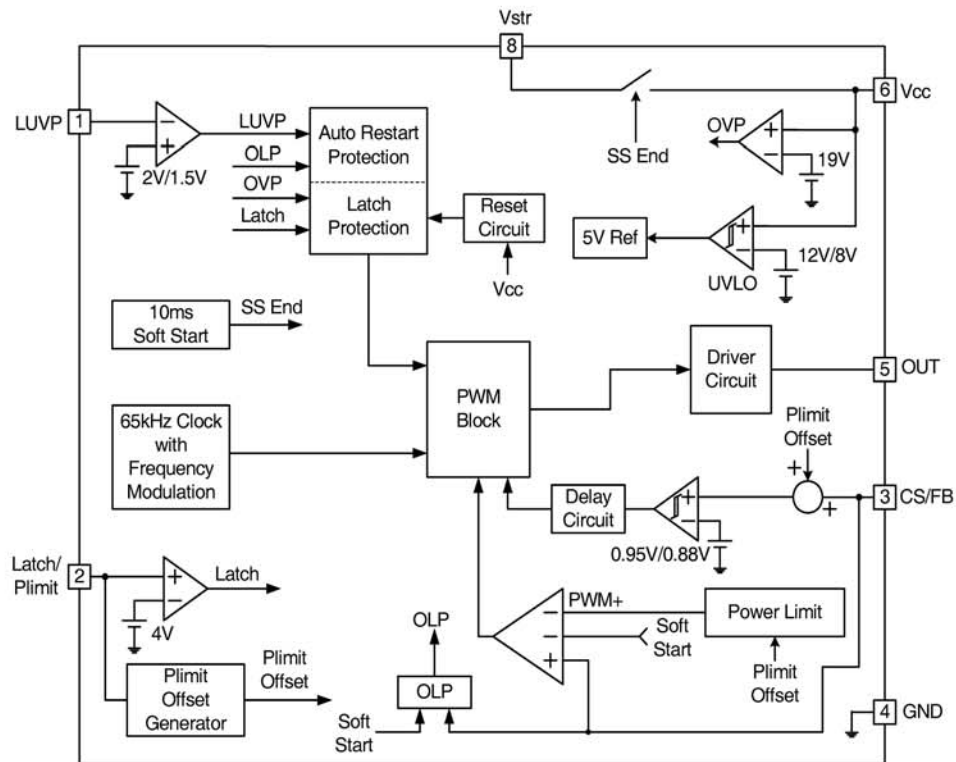


Figure 2. Functional Block Diagram of FAN7602

Pin Assignments

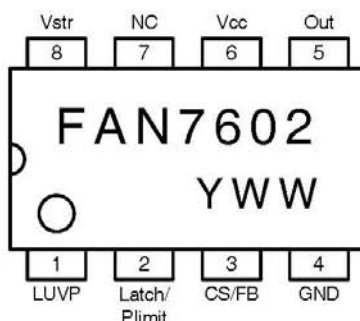


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	LUVP	Line Under Voltage Protection Pin. This pin is used to protect the set when the input voltage is lower than the rated input voltage range.
2	Latch/Plimit	Latch Protection and Power Limit Pin. When the pin voltage exceeds 4V, the latch protection works and the latch protection is reset when the Vcc voltage is lower than 5V. For the power limit function, the OCP level decreases as the pin voltage increases.
3	CS/FB	Current Sense and Feedback Pin. This pin is used to sense the MOSFET current for the current mode PWM and OCP. The output voltage feedback information and the current sense information are added using external RC filter.
4	GND	Ground Pin. This pin is used for the ground potential of all the pins. For proper operation, the signal ground and the power ground should be separated.
5	OUT	Gate Drive Output Pin. This pin is an output pin to drive an external MOSFET. The peak sourcing current is 450mA and the peak sinking current is 600mA. For proper operation, the stray inductance in the gate driving path must be minimized.
6	Vcc	Supply Voltage Pin. IC operating current and MOSFET driving current are supplied using this pin.
7	NC	No Connection.
8	Vstr	Start-up Pin. This pin is used to supply IC operating current during IC start-up. After start-up, the internal JFET is turned off to reduce power loss.

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table defines the conditions for actual device operation.

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	20	V
I _{OH} , I _{OL}	Peak Drive Output Current	+450/-600	mA
V _{CS,FB}	CS/FB Input Voltage	-0.3 to 20	V
V _{LUVP}	LUVP Input Voltage	-0.3 to 10	V
V _{Latch}	Latch/Plimit Input Voltage	-0.3 to 10	V
V _{str}	Vstr Input Voltage	600	V
T _J	Operating Junction Temperature	150	°C
T _{opr}	Operating Temperature Range	-25 to 125	°C
T _{stg}	Storage Temperature Range	-55 to 150	°C
P _D	Power Dissipation	1.2	W
V _{ESD_HBM}	ESD Capability, Human Body Model	2.0	kV
V _{ESD_MM}	ESD Capability, Machine Model	300	V
V _{ESD_CDM}	ESD Capability, Charged Device Model	500	V

Thermal Impedance

Symbol	Parameter	Value	Unit
R _{θja}	Thermal Resistance, Junction to Ambient	8-DIP	100 °C/W

Note:

- Regarding the test environment and PCB type, please refer to JESD51-2 and JESD51-10.

Electrical Characteristics(V_{CC} = 14V, T_A = -25°C~125°C, unless otherwise specified)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
START UP SECTION						
I _{str}	V _{str} Start-up Current	V _{str} = 30V, T _A = 25°C	0.7	1	1.4	mA
UNDER VOLTAGE LOCK OUT SECTION						
V _{th(start)}	Start Threshold Voltage	V _{CC} increasing	11	12	13	V
V _{th(stop)}	Stop Threshold Voltage	V _{CC} decreasing	7	8	9	V
HY(uvlo)	UVLO Hysteresis		3.6	4	4.4	V
SUPPLY CURRENT SECTION						
I _{st}	Start-up Supply Current	T _A = 25°C	-	250	320	μA
I _{cc}	Operating Supply Current	Output no switching	-	1	1.5	mA
SOFT START SECTION						
T _{ss}	Soft Start Time ⁽¹⁾		5	10	15	ms
PWM SECTION						
F _{OSC}	Operating Frequency	V _{CS/FB} = 0.2V, T _A = 25°C	59	65	73	kHz
ΔF	Frequency Modulation		-	±2	-	kHz
V _{CS/FB1}	CS/FB Threshold Voltage	T _A = 25°C	0.9	1.0	1.1	V
T _D	Propagation Delay to Output ⁽¹⁾		-	100	150	ns
D _{MAX}	Maximum Duty Cycle		70	75	80	%
D _{MIN}	Minimum Duty Cycle		-	-	0	%
BURST MODE SECTION						
V _{CS/FB2}	Burst On Threshold Voltage	T _A = 25°C	0.84	0.95	1.06	V
V _{CS/FB3}	Burst Off Threshold Voltage	T _A = 25°C	0.77	0.88	0.99	V
POWER LIMIT SECTION						
K _{Plimit}	Offset Gain	V _{Latch/Plimit} = 2V, T _A = 25°C	0.12	0.16	0.20	
OUTPUT SECTION						
V _{OH}	Output Voltage High	T _A = 25°C, I _{source} = 100mA	11.5	12	14	V
V _{OL}	Output Voltage Low	T _A = 25°C, I _{sink} = 100mA	-	1	2.5	V
T _r	Rising Time ⁽¹⁾	T _A = 25°C, C _l = 1nF	-	45	150	ns
T _f	Falling Time ⁽¹⁾	T _A = 25°C, C _l = 1nF	-	35	150	ns

Note:

- These parameters, although guaranteed by design, are not tested in mass production.

Electrical Characteristics (Continued)(V_{CC} = 14V, T_A = -25°C~125°C, unless otherwise specified)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
PROTECTION SECTION						
V _{Latch}	Latch Voltage		3.6	4	4.4	V
T _{OLP}	Overload Protection Time ⁽¹⁾		20	22	24	ms
T _{OLP_ST}	Overload Protection Time at Start-up		30	37	44	ms
V _{OLP}	Overload Protection Level		-	0	0.1	V
V _{LUVPOff}	Line Under-Voltage Protection On to Off	T _A = 25°C	1.9	2	2.1	V
V _{LUVPOn}	Line Under-Voltage Protection Off to On	T _A = 25°C	1.4	1.5	1.6	V
V _{OVP}	Over Voltage Protection	T _A = 25°C	18	19	20	V

Note:

1. These parameters, although guaranteed by design, are not tested in mass production.

Applications Information

1. Start-up Circuit and Soft Start Block

The FAN7602 contains a start-up switch to reduce the power loss of the external start-up circuit of the conventional PWM converters. The internal start-up circuit charges the Vcc capacitor with 0.9mA current source if the AC line is connected. The start-up switch is turned off 15ms after IC starts up, as shown in Fig. 19. The soft-start function starts when the Vcc voltage reaches the start threshold voltage of 12V and ends when the internal soft-start voltage reaches 1V. The internal start-up circuit starts charging the Vcc capacitor again if the Vcc voltage is lowered to the minimum operating voltage, 8V. The UVLO block shuts down the output drive circuit and some blocks to reduce the IC operating current and the internal soft-start voltage drops to zero. If the Vcc voltage reaches the start threshold voltage, the IC starts switching again and the soft start block works as well.

During the soft start, pulse-width modulated (PWM) comparator compares the CS/FB pin voltage with the soft start voltage. The soft-start voltage starts from 0.5V and the soft-start ends when it reaches 1V and the soft-start time is 10ms. The start-up switch is turned off when the soft start voltage reaches 1.5V.

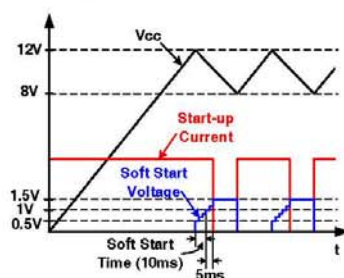


Figure 19. Start-up Current and Vcc Voltage

2. Oscillator Block

The oscillator frequency is set internally and a frequency modulation (FM) function reduces EMI. The average frequency is 65kHz and the modulation frequency is ± 2 kHz. The frequency varies from 63kHz to 67kHz with 16 steps. The frequency step is 250Hz and FM frequency is 125Hz, as shown in Fig. 20.

3. Current Sense and Feedback Block

The FAN7602 performs the current sensing for the current mode PWM and the output voltage feedback with only one pin, pin3. To achieve the two functions with one pin, an internal LEB (leading edge blanking) circuit to filter the current sense noise is not included because the external RC filter is necessary to add the output voltage

feedback information and the current sense information. Fig. 21 shows the current sense and feedback circuits. R_S is the current sense resistor to sense the switch current. The current sense information is filtered by an RC filter composed of R_F and C_F . According to the output voltage feedback information, I_{FB} charges or stops charging C_F to adjust the offset voltage. If I_{FB} is zero, C_F is discharged through R_F and R_S to lower the offset voltage.

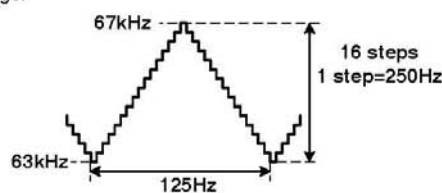


Figure 20. Frequency Modulation

Figure 22 shows typical voltage waveforms of the CS/FB pin. The current sense waveform is added to the offset voltage as shown in the figure. The CS/FB pin voltage is compared with PWM+, that is 1V - Plimit offset as shown in Fig. 22. If the CS/FB voltage meets PWM+, the output drive is shut off. As shown in Fig. 22, if the feedback offset voltage is low, the switch on time is increased. If the feedback offset voltage is high, then the switch on time is decreased. In this way, the duty cycle is controlled according to the output load condition. In general, the maximum output power increases as the input voltage increases because the current slope during switch on-time increases. To limit the output power of the converter constantly, the power limit function is included in the FAN7602. Sensing the converter input voltage through the Latch/Plimit pin, the Plimit offset voltage is subtracted from 1V. As shown in Fig. 22, the Plimit offset voltage is subtracted from 1V and the switch on-time decreases as the Plimit offset voltage increases. If the converter input voltage increases, the switch on-time decreases, controlling the output power constant. The offset voltage is proportional to the Latch/Plimit pin voltage and the gain is 0.16; if the Latch/Plimit voltage is 1V, the offset voltage is 0.16V.

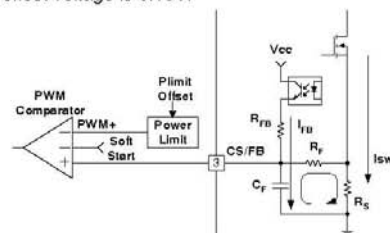


Figure 21. Current Sense and Feedback Circuits

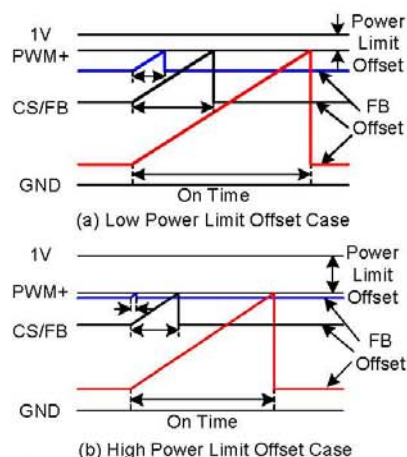


Figure 22. CS/FB Pin Voltage Waveforms

4. Burst Mode Block

The FAN7602 contains the burst mode block to reduce the power loss at a light load and no load as the FAN7601. A hysteresis comparator senses the offset voltage of the Burst+ for the burst mode as shown in Fig. 23. The Burst+ is the sum of the CS/FB voltage and Plimit offset voltage. The FAN7602 enters the burst mode when the offset voltage of the Burst+ is higher than 0.95V and exits the burst mode when the offset voltage is lower than 0.88V. The offset voltage is sensed during the switch off time.

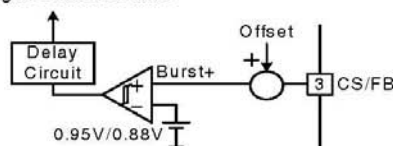


Figure 23. Burst Mode Block

5. Protection Block

The FAN7602 contains several protection functions to improve system reliability.

5.1 Overload Protection (OLP)

The FAN7602 contains the overload protection function. If the output load is higher than the rated output current, the output voltage drops and the feedback error amplifier is saturated. The offset of the CS/FB voltage representing the feedback information is almost zero. As shown in Fig. 24, the CS/FB voltage is compared with 50mV reference when the internal clock signal is high and, if the voltage is lower than 50mV, the OLP timer starts count-

ing. If the OLP condition persists for 22ms, the timer generates the OLP signal. And this protection is reset by the UVLO. The OLP block is enabled after the soft start finishes.

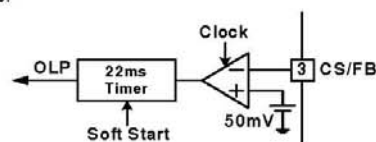


Figure 24. Overload Protection Circuit

5.2 Line Under Voltage Protection

If the input voltage of the converter is lower than the minimum operating voltage, the converter input current increases too much, causing component failure. Therefore, if the input voltage is low, the converter should be protected. In the FAN7602, the LUVVP circuit senses the input voltage using the LUVVP pin and, if this voltage is lower than 2V, the LUVVP signal is generated. The comparator has 0.5V hysteresis. If the LUVVP signal is generated, the output drive block is shut down, the output voltage feedback loop is saturated, and the OLP works if the LUVVP condition persists more than 22ms.

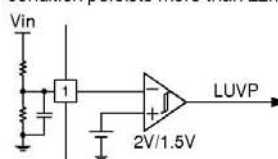


Figure 25. Line UVP Circuit

5.3 Latch Protection

The latch protection is provided to protect the system against abnormal conditions using the Latch/Plimit pin. The Latch/Plimit pin can be used for the output over-voltage protection and/or other protections. If the Latch/Plimit pin voltage is made higher than 4V by an external circuit, the IC is shut down. The latch protection is reset when the Vcc voltage is lower than 5V.

5.4 Over-Voltage Protection (OVP)

If the Vcc voltage reaches 19V, the IC shuts down and the OVP protection is reset when the Vcc voltage is lower than 5V.

6. Output Drive Block

The FAN7602 contains a single totem-pole output stage to drive a power MOSFET. The drive output is capable of up to 450mA sourcing current and 600mA sinking current with typical rise and fall time of 45ns, 35ns respectively with a 1nF load.

**L6562**

TRANSITION-MODE PFC CONTROLLER

1 Features

- REALISED IN BCD TECHNOLOGY
- TRANSITION-MODE CONTROL OF PFC PRE-REGULATORS
- PROPRIETARY MULTIPLIER DESIGN FOR MINIMUM THD OF AC INPUT CURRENT
- VERY PRECISE ADJUSTABLE OUTPUT OVERVOLTAGE PROTECTION
- ULTRA-LOW ($\leq 70\mu\text{A}$) START-UP CURRENT
- LOW ($\leq 4\text{ mA}$) QUIESCENT CURRENT
- EXTENDED IC SUPPLY VOLTAGE RANGE
- ON-CHIP FILTER ON CURRENT SENSE
- DISABLE FUNCTION
- 1% (@ $T_j = 25^\circ\text{C}$) INTERNAL REFERENCE VOLTAGE
- -600/+800mA TOTEM POLE GATE DRIVER WITH UVLO PULL-DOWN AND VOLTAGE CLAMP
- DIP-8/SO-8 PACKAGES ECOPACK®

1.1 APPLICATIONS

- PFC PRE-REGULATORS FOR:
 - IEC61000-3-2 COMPLIANT SMPS (TV,

Figure 1. Packages



Table 1. Order Codes

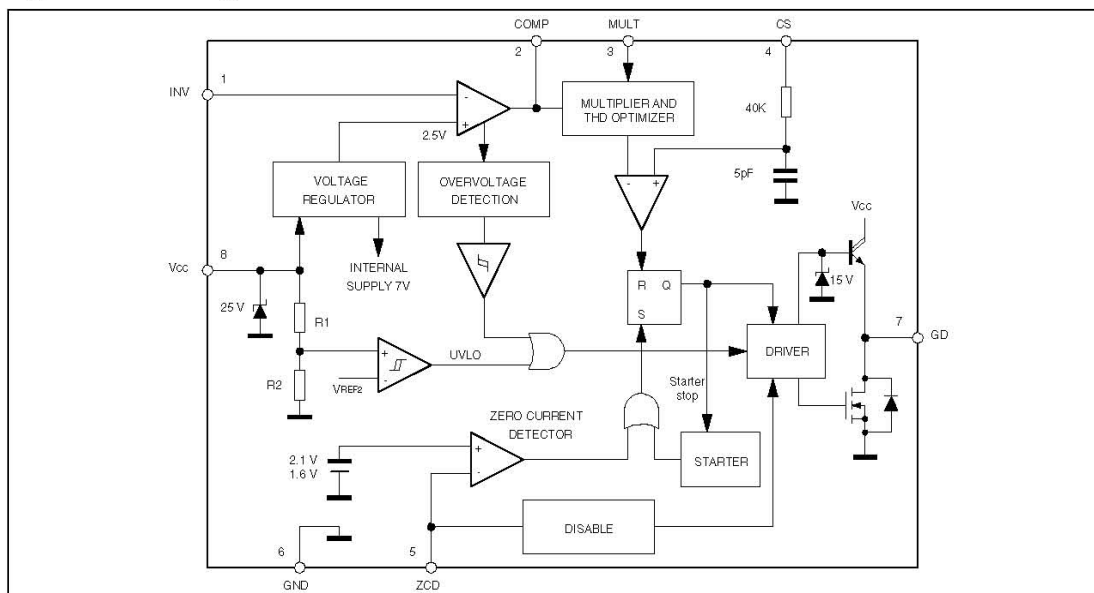
Part Number	Package
L6562N	DIP-8
L6562D	SO-8
L6562DTR	Tape & Reel

- DESKTOP PC, MONITOR) UP TO 300W
- HI-END AC-DC ADAPTER/CHARGER
 - ENTRY LEVEL SERVER & WEB SERVER

2 Description

The L6562 is a current-mode PFC controller operating in Transition Mode (TM). Pin-to-pin compatible with the predecessor L6561, it offers improved performance.

Figure 2. Block Diagram



2 Description (continued)

The highly linear multiplier includes a special circuit, able to reduce AC input current distortion, that allows wide-range-mains operation with an extremely low THD, even over a large load range.

The output voltage is controlled by means of a voltage-mode error amplifier and a precise (1% @T_J = 25°C) internal voltage reference.

The device features extremely low consumption ($\leq 70 \mu\text{A}$ before start-up and $< 4 \text{ mA}$ running) and includes a disable function suitable for IC remote ON/OFF, which makes it easier to comply with energy saving norms (Blue Angel, EnergyStar, Energy2000, etc.).

An effective two-step OVP enables to safely handle overvoltages either occurring at start-up or resulting from load disconnection.

The totem-pole output stage, capable of 600 mA source and 800 mA sink current, is suitable for big MOS-FET or IGBT drive which, combined with the other features, makes the device an excellent low-cost solution for EN61000-3-2 compliant SMPS's up to 300W.

Table 2. Absolute Maximum Ratings

Symbol	Pin	Parameter	Value	Unit
V _{CC}	8	IC Supply voltage (I _{CC} = 20 mA)	self-limited	V
---	1 to 4	Analog Inputs & Outputs	-0.3 to 8	V
I _{ZCD}	5	Zero Current Detector Max. Current	-50 (source) 10 (sink)	mA
P _{tot}		Power Dissipation @T _{amb} = 50°C (DIP-8) (SO-8)	1 0.65	W
T _J		Junction Temperature Operating range	-40 to 150	°C
T _{stg}		Storage Temperature	-55 to 150	°C

Figure 3. Pin Connection (Top view)

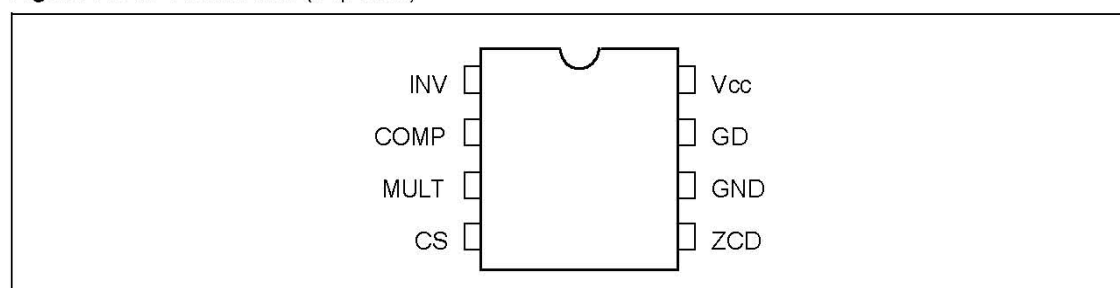


Table 3. Thermal Data

Symbol	Parameter	SO8	Minidip	Unit
R _{th j-amb}	Max. Thermal Resistance, Junction-to-ambient	150	100	°C/W

Table 4. Pin Description

N°	Pin	Function
1	INV	Inverting input of the error amplifier. The information on the output voltage of the PFC pre-regulator is fed into the pin through a resistor divider.
2	COMP	Output of the error amplifier. A compensation network is placed between this pin and INV (pin #1) to achieve stability of the voltage control loop and ensure high power factor and low THD.
3	MULT	Main input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop.
4	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal sinusoidal-shaped reference, generated by the multiplier, to determine MOSFET's turn-off.
5	ZCD	Boost inductor's demagnetization sensing input for transition-mode operation. A negative-going edge triggers MOSFET's turn-on.
6	GND	Ground. Current return for both the signal part of the IC and the gate driver.
7	GD	Gate driver output. The totem pole output stage is able to drive power MOSFET's and IGBT's with a peak current of 600 mA source and 800 mA sink. The high-level voltage of this pin is clamped at about 12V to avoid excessive gate voltages in case the pin is supplied with a high V _{CC} .
8	V _{CC}	Supply Voltage of both the signal part of the IC and the gate driver. The supply voltage upper limit is extended to 22V min. to provide more headroom for supply voltage changes.

Table 5. Electrical Characteristics

(T_J = -25 to 125°C, V_{CC} = 12, C_O = 1 nF; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE						
V _{CC}	Operating range	After turn-on	10.3		22	V
V _{CCOn}	Turn-on threshold	(1)	11	12	13	V
V _{CCOff}	Turn-off threshold	(1)	8.7	9.5	10.3	V
Hys	Hysteresis		2.2		2.8	V
V _Z	Zener Voltage	I _{CC} = 20 mA	22	25	28	V
SUPPLY CURRENT						
I _{start-up}	Start-up Current	Before turn-on, V _{CC} = 11V		40	70	μA
I _q	Quiescent Current	After turn-on		2.5	3.75	mA
I _{CC}	Operating Supply Current	@ 70 kHz		3.5	5	mA
I _q	Quiescent Current	During OVP (either static or dynamic) or V _{ZCD} = 150 mV			2.2	mA
MULTIPLIER INPUT						
I _{MULT}	Input Bias Current	V _{VFF} = 0 to 4 V			-1	μA
V _{MULT}	Linear Operation Range		0 to 3			V
$\frac{\Delta V_{CS}}{\Delta V_{MULT}}$	Output Max. Slope	V _{MULT} = 0 to 0.5V V _{COMP} = Upper clamp	1.65	1.9		V/V
K	Gain (2)	V _{MULT} = 1 V, V _{COMP} = 4 V	0.5	0.6	0.7	1/V
ERROR AMPLIFIER						
V _{INV}	Voltage Feedback Input Threshold	T _J = 25 °C	2.465	2.5	2.535	V
		10.3 V < V _{CC} < 22 V (1)	2.44		2.56	
	Line Regulation	V _{CC} = 10.3 V to 22V		2	5	mV
I _{INV}	Input Bias Current	V _{INV} = 0 to 3 V			-1	μA

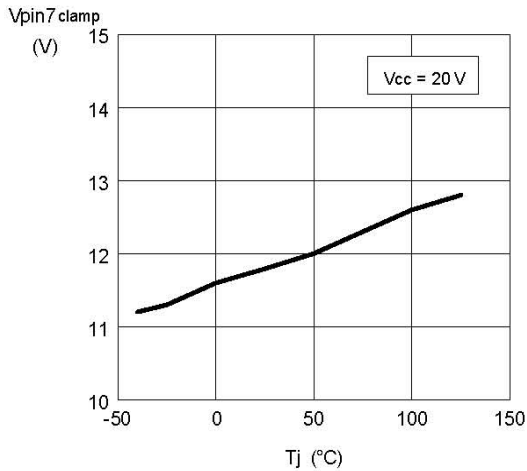
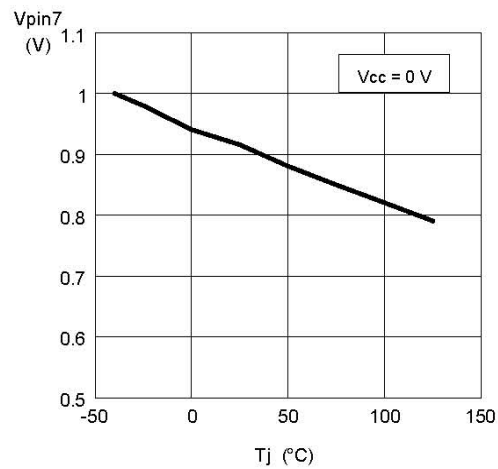
Table 5. Electrical Characteristics (continued)(T_j = -25 to 125°C, V_{CC} = 12, C_O = 1 nF; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G _v	Voltage Gain	Open loop	60	80		dB
GB	Gain-Bandwidth Product			1		MHz
I _{COMP}	Source Current	V _{COMP} = 4V, V _{INV} = 2.4 V	-2	-3.5	-5	mA
	Sink Current	V _{COMP} = 4V, V _{INV} = 2.6 V	2.5	4.5		mA
V _{COMP}	Upper Clamp Voltage	I _{SOURCE} = 0.5 mA	5.3	5.7	6	V
	Lower Clamp Voltage	I _{SINK} = 0.5 mA (1)	2.1	2.25	2.4	V
CURRENT SENSE COMPARATOR						
I _{CS}	Input Bias Current	V _{CS} = 0			-1	μA
t _{d(H-L)}	Delay to Output			200	350	ns
V _{CS clamp}	Current sense reference clamp	V _{COMP} = Upper clamp	1.6	1.7	1.8	V
V _{CSoffset}	Current sense offset	V _{MULT} = 0		30		mV
		V _{MULT} = 2.5V		5		
ZERO CURRENT DETECTOR						
V _{ZCDH}	Upper Clamp Voltage	I _{ZCD} = 2.5 mA	5.0	5.7	6.5	V
V _{ZCDL}	Lower Clamp Voltage	I _{ZCD} = -2.5 mA	0.3	0.65	1	V
V _{ZCDA}	Arming Voltage (positive-going edge)	(3)		2.1		V
V _{ZCDT}	Triggering Voltage (negative-going edge)	(3)		1.6		V
I _{ZCDB}	Input Bias Current	V _{ZCD} = 1 to 4.5 V		2		μA
I _{ZCDsrc}	Source Current Capability		-2.5		-5.5	mA
I _{ZCDsnk}	Sink Current Capability		2.5			mA
V _{ZCDdis}	Disable threshold		150	200	250	mV
V _{ZCDen}	Restart threshold				350	mV
I _{ZCDres}	Restart Current after Disable		30	75		μA
STARTER						
t _{START}	Start Timer period		75	130	300	μs
OUTPUT OVERVOLTAGE						
I _{OVP}	Dynamic OVP triggering current		35	40	45	μA
Hys	Hysteresis	(3)		30		μA
	Static OVP threshold	(1)	2.1	2.25	2.4	V
GATE DRIVER						
V _{OH}	Dropout Voltage	I _{GDsource} = 20 mA		2	2.6	
		I _{GDsource} = 200 mA		2.5	3	V
V _{OL}		I _{GDsink} = 200 mA		0.9	1.9	V
t _f	Voltage Fall Time			30	70	ns
t _r	Voltage Rise Time			40	80	ns
V _{Oclamp}	Output clamp voltage	I _{GDsource} = 5mA; V _{CC} = 20V	10	12	15	V
	UVLO saturation	V _{CC} = 0 to V _{CCon} , I _{sink} =10mA			1.1	V

(1) All parameters are in tracking

(2) The multiplier output is given by: V_{CS} = K · V_{MULT} · (V_{COMP} - 2.5)

(3) Parameters guaranteed by design, functionality tested in production.

Figure 20. Gate-drive clamp vs. T_j Figure 21. UVLO saturation vs. T_j 

4 Application Information

4.1 Overvoltage protection

Under steady-state conditions, the voltage control loop keeps the output voltage V_o of a PFC pre-regulator close to its nominal value, set by the resistors R_1 and R_2 of the output divider. Neglecting ripple components, the current through R_1 , I_{R1} , equals that through R_2 , I_{R2} . Considering that the non-inverting input of the error amplifier is internally referenced at 2.5V, also the voltage at pin INV will be 2.5V, then:

$$I_{R2} = \frac{2.5}{R_2} = I_{R1} = \frac{V_o - 2.5}{R_1}.$$

If the output voltage experiences an abrupt change $\Delta V_o > 0$ due to a load drop, the voltage at pin INV will be kept at 2.5V by the local feedback of the error amplifier, a network connected between pins INV and COMP that introduces a long time constant to achieve high PF (this is why ΔV_o can be large). As a result, the current through R_2 will remain equal to $2.5/R_2$ but that through R_1 will become:

$$I'_{R1} = \frac{V_o - 2.5 + \Delta V_o}{R_1}.$$

The difference current $\Delta I_{R1} = I'_{R1} - I_{R2} = I'_{R1} - I_{R1} = \Delta V_o / R_1$ will flow through the compensation network and enter the error amplifier output (pin COMP). This current is monitored inside the L6562 and if it reaches about 37 μA the output voltage of the multiplier is forced to decrease, thus smoothly reducing the energy delivered to the output. As the current exceeds 40 μA , the OVP is triggered (Dynamic OVP): the gate-drive is forced low to switch off the external power transistor and the IC put in an idle state. This condition is maintained until the current falls below approximately 10 μA , which re-enables the internal starter and allows switching to restart. The output ΔV_o that is able to trigger the Dynamic OVP function is then:

$$\Delta V_o = R_1 \cdot 40 \cdot 10^{-6}.$$

An important advantage of this technique is that the OV level can be set independently of the regulated output voltage: the latter depends on the ratio of R_1 to R_2 , the former on the individual value of R_1 . Another advantage is the precision: the tolerance of the detection current is 12%, that is 12% tolerance on ΔV_o . Since $\Delta V_o \ll V_o$, the tolerance on the absolute value will be proportionally reduced.

Example: $V_o = 400 V$, $\Delta V_o = 40 V$. Then: $R_1 = 40V / 40\mu A = 1M\Omega$; $R_2 = 1M\Omega \cdot 2.5 / (400 - 2.5) = 6.289k\Omega$. The tolerance on the OVP level due to the L6562 will be $40 \cdot 0.12 = 4.8V$, that is 1.2% of the regulated value.

When the load of a PFC pre-regulator is very low, the output voltage tends to stay steadily above the nominal value, which cannot be handled by the Dynamic OVP. If this occurs, however, the error amplifier output will saturate low; hence, when this is detected, the external power transistor is switched off and the IC put in an idle state (Static OVP). Normal operation is resumed as the error amplifier goes back into its linear region. As a result, the L6562 will work in burst-mode, with a repetition rate that can be very low.

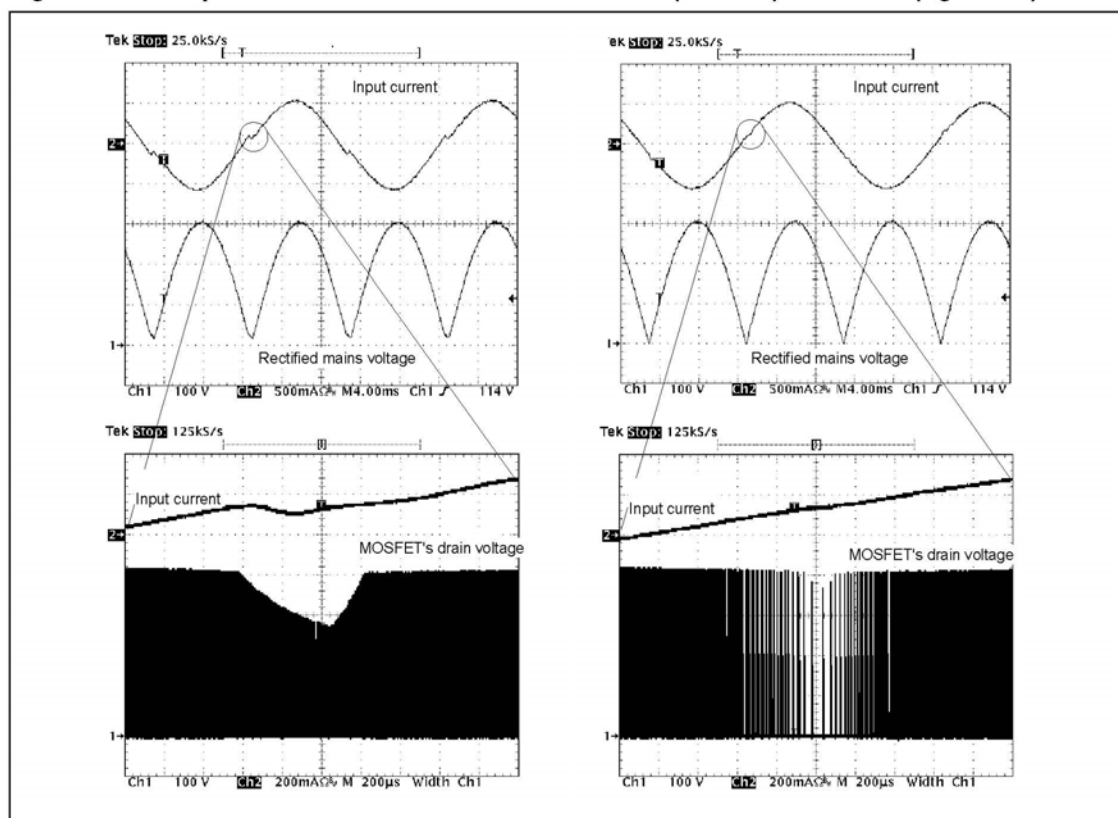
When either OVP is activated the quiescent consumption of the IC is reduced to minimize the discharge of the Vcc capacitor and increase the hold-up capability of the IC supply system.

4.2 THD optimizer circuit

The L6562 is equipped with a special circuit that reduces the conduction dead-angle occurring to the AC input current near the zero-crossings of the line voltage (crossover distortion). In this way the THD (Total Harmonic Distortion) of the current is considerably reduced.

A major cause of this distortion is the inability of the system to transfer energy effectively when the instantaneous line voltage is very low. This effect is magnified by the high-frequency filter capacitor placed after the bridge rectifier, which retains some residual voltage that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop.

Figure 22. THD optimization: standard TM PFC controller (left side) and L6562 (right side)



To overcome this issue the circuit embedded in the L6562 forces the PFC pre-regulator to process more energy near the line voltage zero-crossings as compared to that commanded by the control loop. This will result in both minimizing the time interval where energy transfer is lacking and fully discharging the high-frequency filter capacitor after the bridge. The effect of the circuit is shown in figure 23, where the key waveforms of a standard TM PFC controller are compared to those of the L6562.

Essentially, the circuit artificially increases the ON-time of the power switch with a positive offset added to

the output of the multiplier in the proximity of the line voltage zero-crossings. This offset is reduced as the instantaneous line voltage increases, so that it becomes negligible as the line voltage moves toward the top of the sinusoid.

To maximally benefit from the THD optimizer circuit, the high-frequency filter capacitor after the bridge rectifier should be minimized, compatibly with EMI filtering needs. A large capacitance, in fact, introduces a conduction dead-angle of the AC input current in itself - even with an ideal energy transfer by the PFC pre-regulator - thus making the action of the optimizer circuit little effective.

Figure 23. Typical application circuit (250W, Wide-range mains)

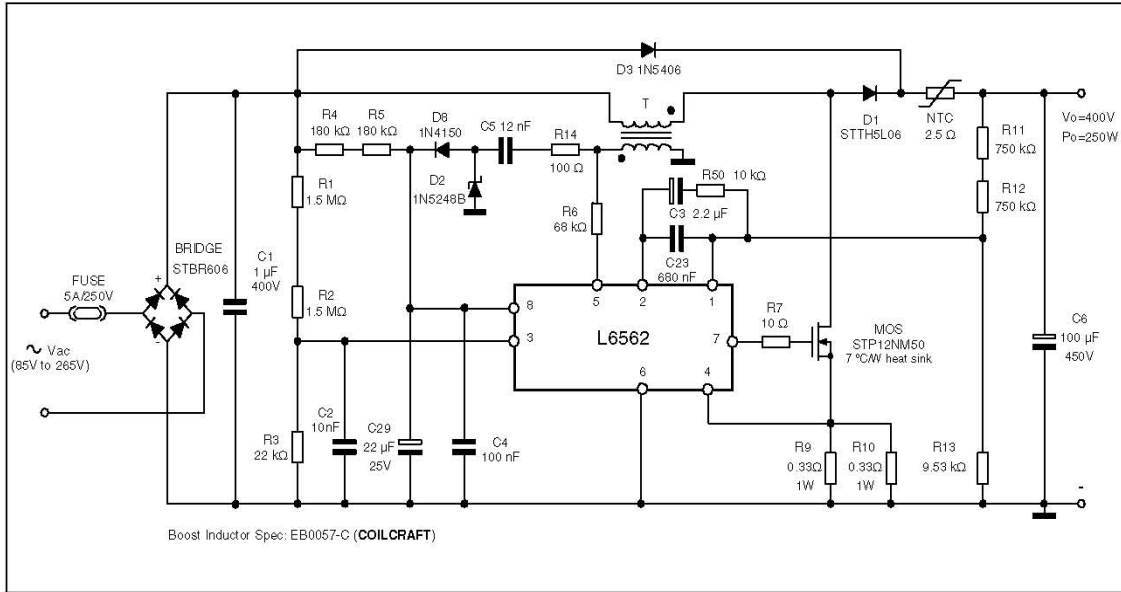
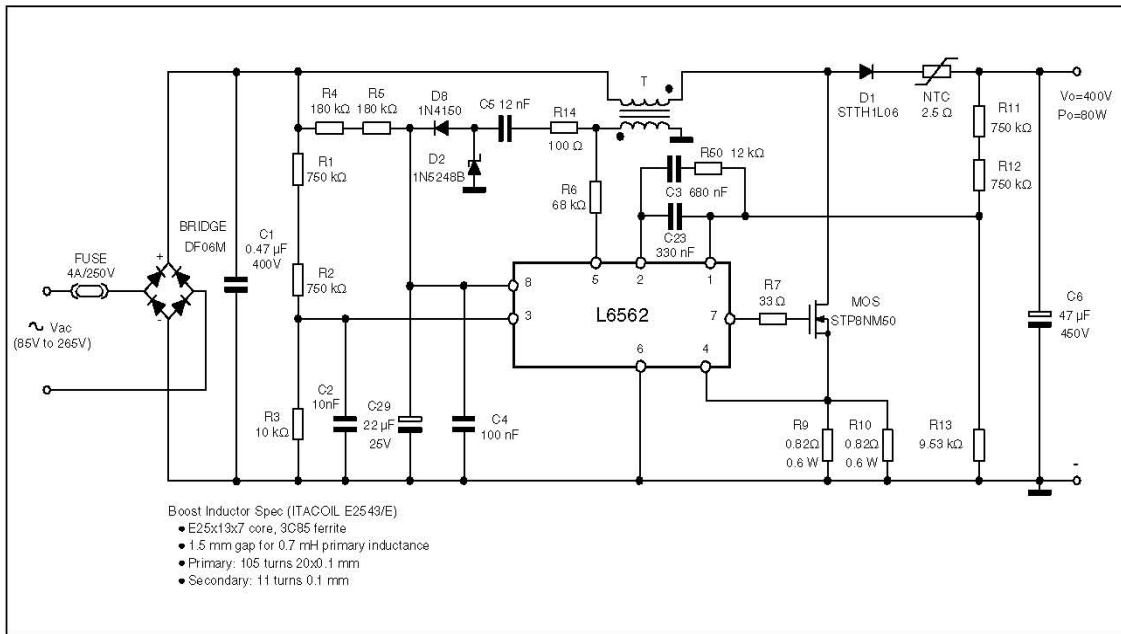


Figure 24. Demo board (EVAL6562-80W, Wide-range mains): Electrical schematic



LM393, LM293, LM2903, LM2903V, NCV2903

Low Offset Voltage Dual Comparators

The LM393 series are dual independent precision voltage comparators capable of single or split supply operation. These devices are designed to permit a common mode range-to-ground level with single supply operation. Input offset voltage specifications as low as 2.0 mV make this device an excellent selection for many applications in consumer, automotive, and industrial electronics.

Features

- Wide Single-Supply Range: 2.0 Vdc to 36 Vdc
- Split-Supply Range: ± 1.0 Vdc to ± 18 Vdc
- Very Low Current Drain Independent of Supply Voltage: 0.4 mA
- Low Input Bias Current: 25 nA
- Low Input Offset Current: 5.0 nA
- Low Input Offset Voltage: 5.0 mV (max) LM293/393
- Input Common Mode Range to Ground Level
- Differential Input Voltage Range Equal to Power Supply Voltage
- Output Voltage Compatible with DTL, ECL, TTL, MOS, and CMOS Logic Levels
- ESD Clamps on the Inputs Increase the Ruggedness of the Device without Affecting Performance
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes
- Pb-Free Packages are Available

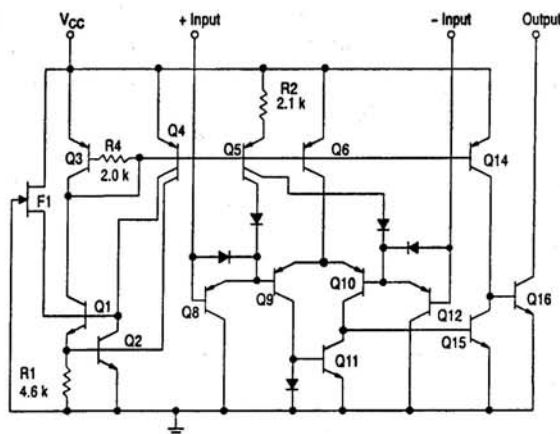
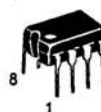


Figure 1. Representative Schematic Diagram
(Diagram shown is for 1 comparator)



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PDIP-8
N SUFFIX
CASE 626

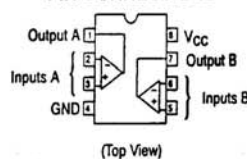


SOIC-8
D SUFFIX
CASE 751



Micro8™
DM SUFFIX
CASE 846A

PIN CONNECTIONS



DEVICE MARKING & ORDERING INFORMATION

See detailed ordering and shipping information and marking information in the package dimensions section on pages 6 and 7 of this data sheet.

LM393, LM293, LM2903, LM2903V, NCV2903

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+36 or ± 18	Vdc
Input Differential Voltage Range	V_{IDR}	36	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to +36	Vdc
Output Short Circuit-to-Ground Output Sink Current (Note 1)	I_{SC} I_{Sink}	Continuous 20	mA
Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D $1/R_{\theta JA}$	570 5.7	mW mW/ $^\circ\text{C}$
Operating Ambient Temperature Range LM293 LM393 LM2903 LM2903V, NCV2903 (Note 2)	T_A	-25 to +85 0 to +70 -40 to +105 -40 to +125	$^\circ\text{C}$
Maximum Operating Junction Temperature LM393, 2903, LM2903V LM293, NCV2903	$T_{J(max)}$	150 150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
ESD Protection at any Pin - Human Body Model - Machine Model	V_{esd}	2000 200	V

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC} , output short circuits to V_{CC} can cause excessive heating and eventual destruction.
2. NCV2903 is qualified for automotive use.

LM393, LM293, LM2903, LM2903V, NCV2903

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+36 or ± 18	Vdc
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JSK4210-022B REPAIR INSTRUCTION

Repair Operation Instruction

