JSK4210-022B SPECIFICATION

Section 目录

深圳晶辰电子科技有限公司 SHENZHEN JEWEL ELECTRONIC & TECHNOLOGY CO.,LTD				DESCRIPTION: 规格书 SPECIFICATION	
THESE SPECIFICATION ARE THE PROPERTY OF JEWEL ELECTRICAL&TECHNOLOGY CO.,LTD ,AND SHALL NOT BE REPRODUCED OR USED AS THE BASIS FOR THE MANUFACTURE OR SELL OF APPARATUSES OR DEVICES WITHOUT PERMISSION.				Model No.: JSK4210-022	
DATE	PREPARED	CHECKED	APPROVED	Document No. JSD20070601	REV:

1. Power Supply Overview 电性能指标：

1.1 Table 1 Input Electrical Characteristics Overview (输入特性）

Input voltage range 输入电压	90Vac-264Vac
Normal voltage range 标准输入	100Vac-240Vac
Frequency range 频率范围	50Hz/60Hz
Max input AC current 满载输入电流	90Vac/3A Max
Inrush current (cold start) 浪涌电流(冷机）	50A/100Vac；100A/240Vac
Efficiency (full load) 效率	80%Min@115Vac,Full load
Harmonic current 谐波电流	GB17625.0-1998/IEC61000-3-2 CALSS D
Leakage Current 泄漏电流	≤0.75mA/220Vac
Standby Power Loss 待机功耗	≤1.0W/220Vac
Input Fuse 输入保险额定值	T5AL/250Vac

1.2 Output Eletrical Characteristics Overview (输出特性）

1.2.1 Table 2 Output Voltage, Current & Regulation. (输出调整率）

Output Voltage 输出电压	Regulation 调整率	Min current 最小电流	Rated current 额定电流
5VSB	±5%	0.1A	1A
5V	±5%	0.2A	2A
24V	±5%	0.2A	5A
12V	±5%	0.1A	2A

1.2.2 Table 3 DC Output Ripple & Noise. (输出波纹和噪声）

Output Voltage	Ripple & Noise(Max)
5VSB	Ripple≤80mV Noise≤150mV
5V	Ripple≤80mV Noise≤150mV
24V	Ripple≤240mV Noise≤500mV
12V	Ripple≤120mV Noise≤240mV

Note: 1)Measurements shall be made with an oscilloscopewith 20Mhz bandwidth .
示波器设置在20MHz带宽

2）Output shall be bypassed at the connector with a 0.1 uF ceramic capacitor and a 10uF electrolytic simulate system loading .
输出并联0.1uF的陶瓷电容和10uF的电解电容。

1.3 On/Off Control (ON/OFF控制）

The power supply DC outputs (without+5.0VSB) shall be enable with a high-level which more than 2.5V.
ON/OFF电平超过2.5V时,电源输出正常。
The+5.0 VSB is on whenever the AC power is present.
只要AC输入，+5VSB就正常输出。

Table 1.

Ps-on Signal	Comments	Outputs
High	≥2.5V	Enable
Low	≤1.5V	Unable
Open		Unable

1.4 Protection:(保护功能）

1.4.1 Table9 DC Over Voltage Protection.(输出过压保护）

Output Voltage	Max. Over Voltage	Comments
24V	30V	Shut off
12V	16V	Shut off

1.4.2 Table 10 DC Output Over current Protection.(输出过流保护）

Output Voltage	Over Current	Comments
5VSB	3-11A	Hiccup
5V	3-11A	Hiccup
24V	8-15A	Shut off
12V	4-9A	Shut off

注:测5VSB之OCP时5V输出须空载，同样测5V之OCP时5VSB输出须空载.

1.4.3 Table 11 DC Output Short Circuit Protection.(输出短路保护）

Output Voltage	Comments
5VSB	Hiccup
5V	Hiccup
24V	Shut off
12V	Shut off

1.4.4 Reset After Shutdown.(保护功能复位）

After power supply enter into shutdown,The power supply will rework after AC reset.

电源进入保护状态后，AC重置后电源才能重新正常工作。

2. Isolation (绝缘性能）

2.1 Table 12 (绝缘性能）

Input To Output	DC500V 4M Min (room temperature)

Note:

2.2 Table 13 (绝缘耐压）

Input To Output	3.0KV/10mA 50Hz 1 minute

Note:

3. Safety (安全规格）

The power supply shall compliance with the following Criterion:

电源安全性满足下列标准

1）GB8898-2001

4. EMC (电磁兼容性）

4.1 EMI（电磁干扰）

The power supply shall compliance with the following Criterion:

电源电磁干扰满足下列规则：

1）Conduction Emission:(传导干扰度）

EN55022， CLASS B

GB9254,CLASS B

* FCC PART15 CLASS B

2) Radiate Emission:(辐射干扰度）

EN55022， CLASS B

GB9254，CLASS B

* FCC PART15 CLASS B

4.2 EMS（电磁干扰）

The power supply shall compliance with the following Criterion:

电源电磁抗干扰满足下列规则：

1）ESD（静电抗扰度）

*GB17626.2-1998/IEC61000-4-2

2) EFT（脉冲群抗扰度）

*GB17626.4-1998/IEC61000-4-4 3KV

3) Surge（雷击浪涌）

*GB17626.5-1998/IEC61000-4-5 2KV/4KV

5. Environmental Requirement（工作环境）

5.1 Temperature（环境温度）

Operating : 0℃ to +40℃

Store: -10℃ to +70℃

5.2 Humidity （环境温度）

Operating : From10% to 90% relative humidity (non-condensing).

Store: From 5 to 95% relative humidity (non-condensing).

5.3 Altitude（海拔高度）

Operating: To10，000ft.

Store: To20，000ft.

5.4 Cooling Method（冷却方式）

Ventilation cooling .

5.5 Vibration (振动耐受）

* 10-55Hz,49.0m/s2(5G),3minutes period, 60minutes each along X, Y and Z axis.

5.6 Impact (冲击耐受）

*196.1m/s2(20G), 11MS, once each X , Y and Z axis.

6.Dimension(物理尺寸）

*210mm x * 130mm x * 30 mm

7.Weight（重量）

*About 540g

备注:带″*″的为参考项.

8.Pin Connection （连接器脚位定义）

Table 14 CON1 Connection And Function

No.	Pin Connection	Function
1	L	AC INPUT L
2	N	AC INPUT N

Note: CON1 Pitch 3.96mm (三PIN中空,针脚180°直脚)

Table 15 CON2 CON5 Connection And Function

No.	Pin Connection	Function
1	GND	GND
2	GND	GND
3	GND	GND
4	GND	GND
5	GND	GND
6	24V	24V
7	24V	24V
8	24V	24V
9	24V	24V
10	24V	24V

Note: CON2 CON5 Pitch 2.5mm (针脚180°直脚)

Table 16 CON3 Connection And Function

No.	Pin Connection	Function
1	GND	GND
2	12V	12V
3	GND	GND
4	12V	12V

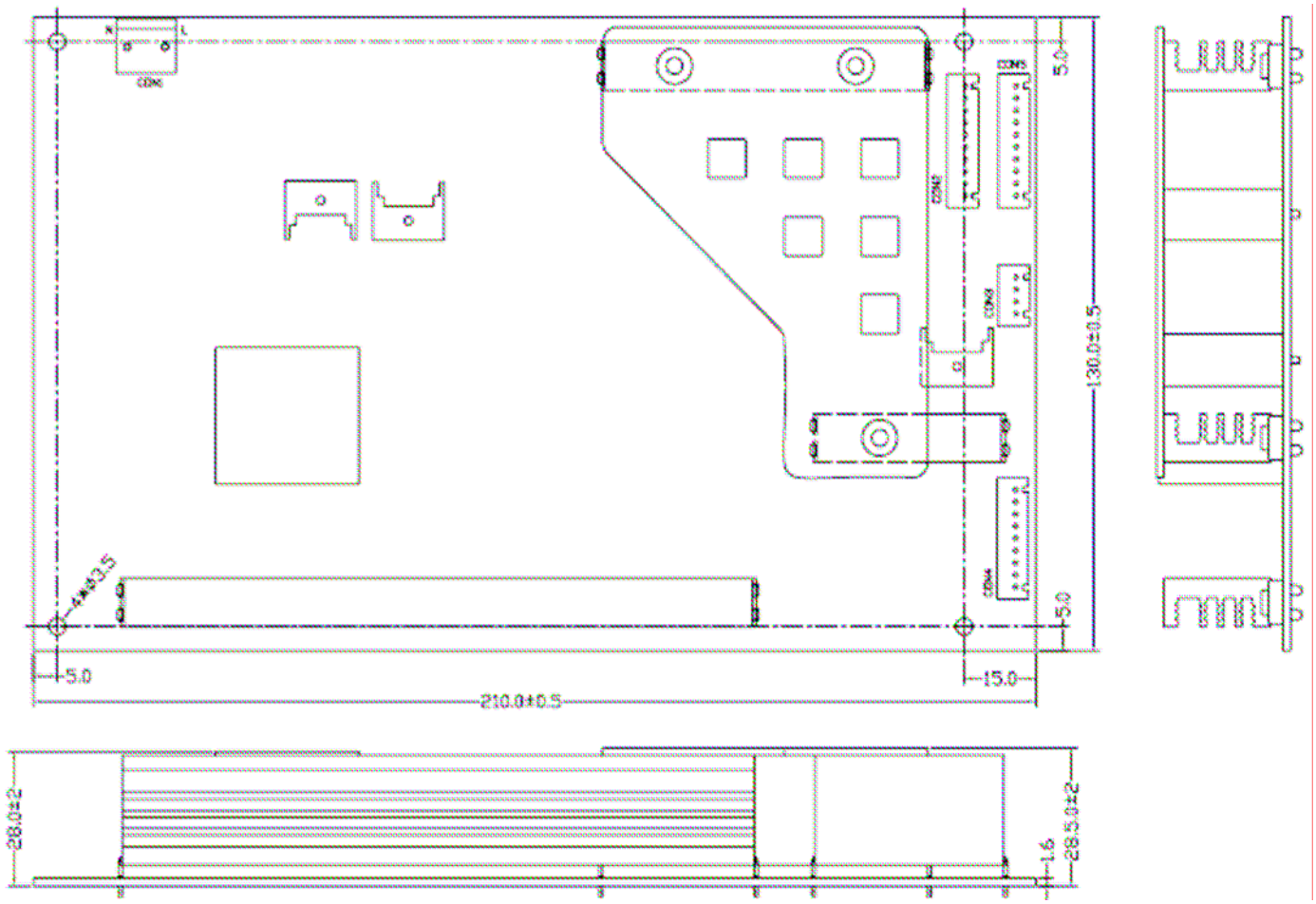
Note: CON3 Pitch:2.5mm (针脚180°直脚)

Table 17 CON4 Connection And Function

No	Pin Connection	Function
1	GND	GND
2	GND	GND
3	GND	GND
4	5V	5V
5	5V	5V
6	5V	5V
7	GND	GND
8	5VSB	5VSB
9	PS-ON	PS-ON

Note: CON4 Pitch:2.5mm (针脚180°直脚)

9. Power Supply mounting (安装尺寸）



深圳晶辰电子科技有限公司 SHENZHEN JEWEL ELECTRONIC & TECHNOLOGY CO.,LTD				DESCRIPTION: 规格书 SPECIFICATION	
THESE SPECIFICATION ARE THE PROPERTY OF JEWEL ELECTRICAL&TECHNOLOGY CO.,LTD ,AND SHALL NOT BE REPRODUCED OR USED AS THE BASIS FOR THE MANUFACTURE OR SELL OF APPARATUSES OR DEVICES WITHOUT PERMISSION.				Model No.: JSK4210-022	
DATE	PREPARED	CHECKED	APPROVED	Document No. JSD20070601	REV:

10. Packing,Shipping and Storing (包装、运输、贮存)

1、Packing(包装)

Product name, part number, supplier's logo, QC stamp, Pb-free display and date must be printed on the package case.
包装箱上有产品名称、型号、厂家标识、厂家质量部门的检验合格证、制造日期等。

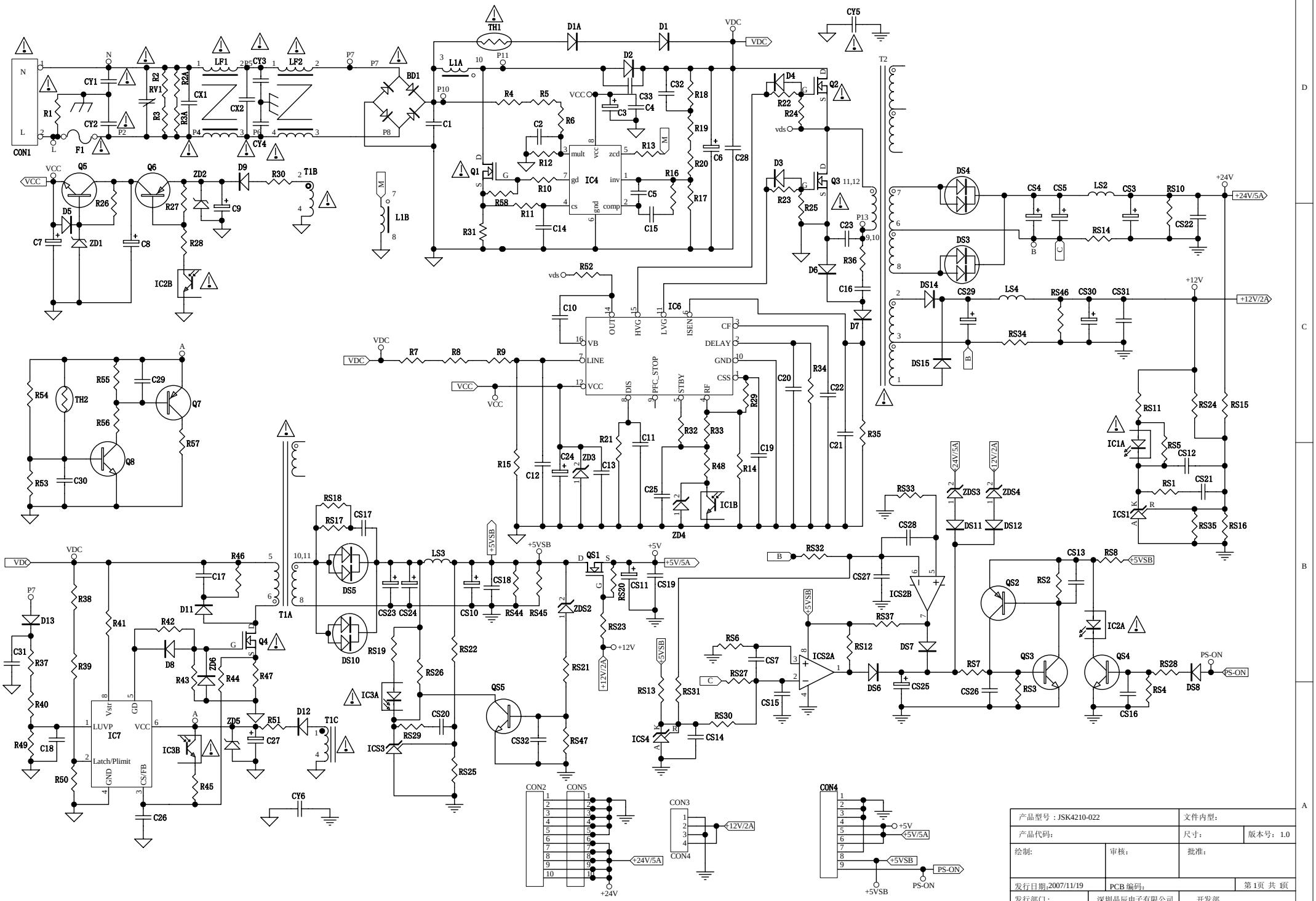
2、Shipping(运输)

This product can be transported through land, sea or air. Measures should be taken for water and sunproof. Also, it should be handled with care
适应于车、船、飞机运输，运输中应遮蓬、防晒、文明装卸。

3、Storing(贮存)

Keep the product staying in the package case before using. The temperature of the stock house should be between -40-+55 C and the humidity should between 5-95%. Keep the product away from hazadous gas, flammable or explosive substances and erosive chemical material. Avoid dramatic vibration or shock and strong magnetic field. The package cases should be racked 20cm above the ground and 50cm away from the wall, window,heat source or ventilation port. Generally the storage term of this product is 2 years. All the products should be doublechecked after that time.
产品未使用时应存放在包装箱内，仓库环境温度为-40℃—55℃，相对湿度为5%—95%，仓库内不允许有有害气体，易燃，易爆的产品及有腐蚀性的化学物品，并且无强烈的机械振动，冲击和强磁场作用，包装箱应垫离地至少20cm高，距离墙壁、热源、窗口或空气入口至少50cm，在本规定条件下的贮存期一般为2年，超过2年后应重新进行检验。

JSK4210-022B SCHEMATIC


CON1
F1
IC4
IC6
IC7
T1A
T1B
T1C
T2
L1A
L1B
BD1
TH1
TH2
VDC
VCC
+24V
+12V
+5V
+5VSB
PS-ON
+24V/5A
+12V/2A
+5V/5A
产品型号：JSK4210-022
文件内型：
产品代码：
尺寸：
版本号：1.0
绘制：
审核：
批准：
发行日期:2007/11/19
PCB 编码：
第 1页 共 1页
发行部门：
深圳晶辰电子有限公司
开发部

JSK4210-022B IC DATASHEETS

IC Characteristic for LCD TV Power Supply

PWM IC(IC6)：L6599

L6599

HIGH-VOLTAGE RESONANT CONTROLLER

TARGET SPEC

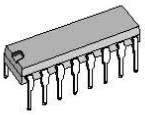
MAIN FEATURES

- 50% DUTY CYCLE, VARIABLE FREQUENCY CONTROL OF RESONANT HALF-BRIDGE
- HIGH-ACCURACY OSCILLATOR
- UP TO 500 kHz OPERATING FREQUENCY
- TWO-LEVEL OCP: FREQUENCY-SHIFT AND LATCHED SHUTDOWN
- INTERFACE WITH PFC CONTROLLER
- LATCHED DISABLE INPUT
- BURST-MODE OPERATION AT LIGHT LOAD
- INPUT FOR POWER-ON/OFF SEQUENCING OR BROWNOUT PROTECTION
- NON-LINEAR SOFT-START FOR MONOTONIC OUTPUT VOLTAGE RISE
- 600V-RAIL COMPATIBLE HIGH-SIDE GATE DRIVER WITH INTEGRATED BOOTSTRAP DIODE AND HIGH dV/dt IMMUNITY
- -300/800 mA HIGH-SIDE AND LOW-SIDE GATE DRIVERS WITH UVLO PULL-DOWN
- DIP16, SO16N PACKAGE

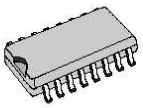
APPLICATIONS

- LCD & PDP TV
- DESKTOP PC, ENTRY-LEVEL SERVER
- TELECOM SMPS
- AC-DC ADAPTER, OPEN FRAME SMPS

BCD OFFLINE TECHNOLOGY



DIP16



SO16N

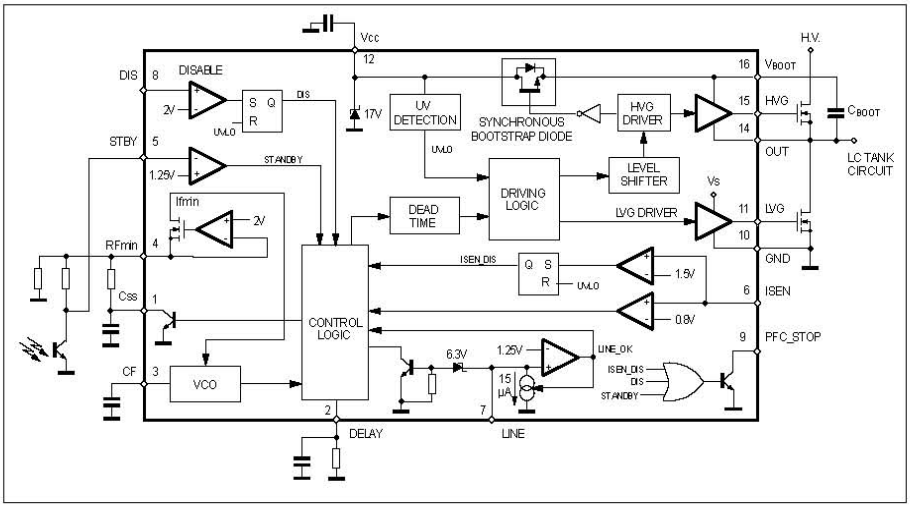
ORDERING NUMBERS:

L6599N **L6599D** **L6599TR**

DESCRIPTION

The L6599 is a double-ended controller specific for the series-resonant half-bridge topology. It provides 50% complementary duty cycle: the high-side switch and the low-side switch are driven ON 180° out-of-phase for exactly the same time. Output voltage regulation is obtained by modulating the operating frequency. A fixed dead-time inserted between the turn-off of one switch

BLOCK DIAGRAM



and the turn-on of the other one guarantees soft-switching and enables high-frequency operation.

To drive the high-side switch with the bootstrap approach, the IC incorporates a high-voltage floating structure able to withstand more than 600V with a synchronous-driven high-voltage DMOS that replaces the external fast-recovery bootstrap diode.

The IC enables the designer to set the operating frequency range of the converter by means of an externally programmable oscillator.

At start-up, to prevent uncontrolled inrush current, the switching frequency starts from a programmable maximum value and progressively decays until it reaches the steady-state value determined by the control loop. This frequency shift is non linear to minimize output voltage overshoots; its duration is programmable as well.

At light load the IC enters a controlled burst-mode operation that keeps the converter input consumption to a minimum.

IC's functions include a not-latched active-low disable input with current hysteresis useful for power sequencing or for brownout protection, a current sense input for OCP with frequency shift and delayed shutdown with automatic restart. A higher level OCP latches off the IC if the first-level protection is not sufficient to control the primary current. Their combination offers complete protection against overload and short circuits. An additional latched disable input (DIS) allows easy implementation of OTP and/or OVP.

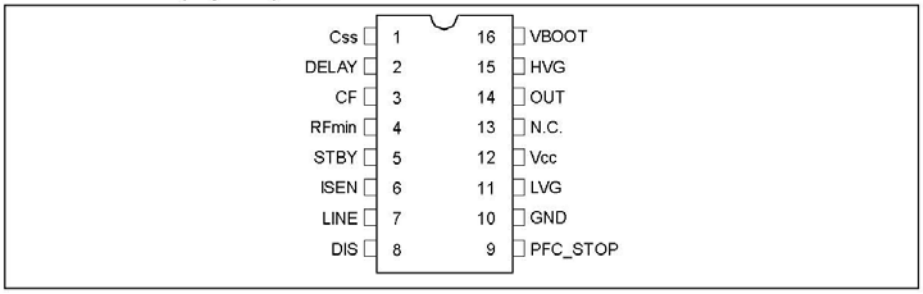
An interface with the PFC controller is provided that enables to switch off the pre-regulator during fault conditions, such as OCP shutdown and DIS high, or during burst-mode operation.

ABSOLUTE MAXIMUM RATINGS

Symbol	Pin	Parameter	Value	Unit
V_{BOOT}	16	Floating supply voltage	-1 to 618	V
V_{OUT}	14	Floating ground voltage	-3 to V_{BOOT}-18	V
dV_{OUT}/dt	14	Floating ground max. slew rate	50	V/ns
Vcc	12	IC Supply voltage (Icc ≤ 25 mA)	Self-limited	V
V_{PFC_STOP}	9	Maximum voltage (pin open)	-0.3 to Vcc	V
I_{PFC_STOP}	9	Maximum sink current (pin low)	Self-limited	A
$V_{LINEmax}$	7	Maximum pin voltage (Ipin ≤ 1mA)	Self-limited	V
I_{RFmin}	4	Maximum source current	2	mA
---	1 to 6, 8	Analog Inputs & Outputs	-0.3 to 5	V
f_{oscmax}		Maximum operating frequency	500	kHz
Ptot		Power Dissipation @Tamb = 70°C (DIP16)	1	W
		Power Dissipation @Tamb = 50°C (SO16)	0.83	
Tj		Junction Temperature Operating range	-40 to 150	°C
Tstg		Storage Temperature	-55 to 150	°C

Note: ESD immunity for pins 14, 15 and 16 is guaranteed up to 900V (Human Body Model)

PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Parameter	Value	Unit
Rth j-amb	Max. Thermal Resistance, Junction-to-ambient (DIP16)	80	°C/W
	Max. Thermal Resistance, Junction-to-ambient (SO16)	120	

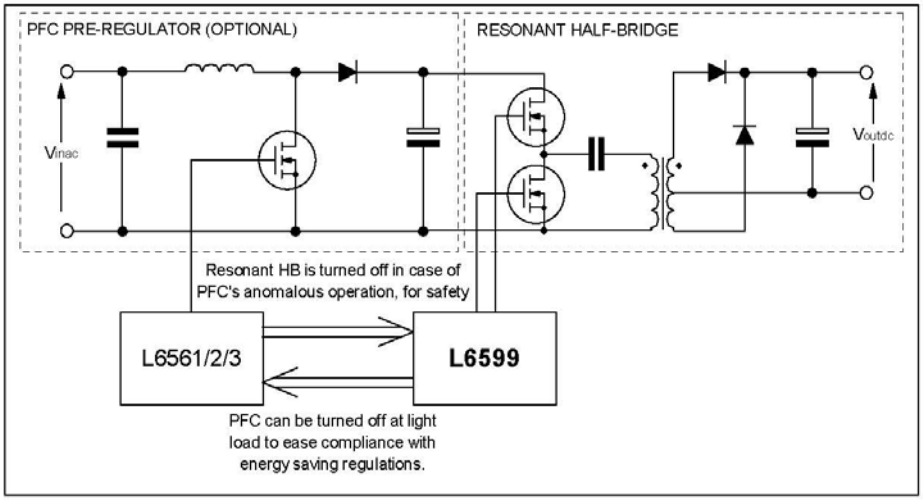
PIN FUNCTIONS

N.	Name	Function
1	Css	Soft start. This pin connects an external capacitor to GND and a resistor to RFmin (pin 4) that set both the maximum oscillator frequency and the time constant for the frequency shift that occurs as the chip starts up (soft-start). An internal switch discharges this capacitor every time the chip turns off (Vcc<UVLO, LINE<1.25 V or >6 V, DIS>2 V, ISEN>1.5 V, DELAY>2 V) to make sure it will be soft-started next, and when the voltage on the current sense pin (ISEN) exceeds 0.8 V, as long as it stays above 0.75V.
2	DELAY	Delayed shutdown upon overcurrent. A capacitor and a resistor are connected from this pin to GND to set the maximum duration of an overcurrent condition before the IC stops switching and the delay after which the IC restarts switching. Every time the voltage on the ISEN pin exceeds 0.8V the capacitor is charged by an internal 150 µA current generator and is slowly discharged by the external resistor. If the voltage on the pin reaches 2 V, the soft start capacitor is completely discharged so that the switching frequency is pushed to its maximum value and the 150 µA is kept always on. As the voltage on the pin exceeds 3.5V the IC stops switching and the internal generator is turned off, so that the voltage on the pin will decay because of the external resistor. The IC will be soft-restarted as the voltage drops below 0.3V. In this way, under short circuit conditions, the converter will work intermittently with very low input average power.
3	CF	Timing capacitor. A capacitor connected from this pin to GND is charged and discharged by internal current generators programmed by the external network connected to pin 4 (RFmin) and determines the switching frequency of the converter.
4	RFmin	Minimum oscillator frequency setting. This pin provides a precise 2V reference and a resistor connected from this pin to GND defines a current that is used to set the minimum oscillator frequency. To close the feedback loop that regulates the converter output voltage by modulating the oscillator frequency, the phototransistor of an optocoupler will be connected to this pin through a resistor. The value of this resistor will set the maximum operating frequency. An R-C series connected from this pin to GND sets frequency shift at start-up to prevent excessive energy inrush (soft-start).
5	STBY	Burst-mode operation threshold. The pin senses some voltage related to the feedback control, which is compared to an internal reference (1.25V). If the voltage on the pin is lower than the reference, the IC enters an idle state and its quiescent current is reduced. The chip restarts switching as the voltage exceeds the reference by 50 mV. Soft-start is not invoked. This function realizes burst-mode operation when the load falls below a level that can be programmed by properly choosing the resistor connecting the optocoupler to pin RFmin (see block diagram). Tie the pin to RFmin if burst-mode is not used.
6	ISEN	Current sense input. The pin senses the primary current though a sense resistor or a capacitive divider for lossless sensing. This input is not intended for a cycle-by-cycle control; hence the voltage signal must be filtered to get average current information. As the voltage exceeds a 0.8 V threshold (with 50 mV hysteresis), the soft-start capacitor connected to pin 1 is internally discharged: the frequency increases hence limiting the power throughput. Under output short circuit, this normally results in a nearly constant peak primary current. This condition is allowed for a maximum time set at pin 2. If the current keeps on building up despite this frequency increase, a second comparator referenced at 1.5 V latches the device off and brings its consumption almost to a "before start-up" level. The information is latched and it is necessary to recycle the supply voltage of the IC to enable it to restart: the latch is removed as the voltage on the Vcc pin goes below the UVLO threshold. Tie the pin to GND if the function is not used.
7	LINE	Line sensing input. The pin is to be connected to the high-voltage input bus with a resistor divider to perform either AC or DC (in systems with PFC) brownout protection. A voltage below 1.25V shuts down (not latched) the IC, lowers its consumption and discharges the soft-start capacitor. IC's operation is re-enabled (soft-started) as the voltage exceeds 1.25V. The comparator is provided with current hysteresis: an internal 15 µA current generator is ON as long as the voltage applied at the pin is below 1.25V and is OFF if this value is exceeded. Bypass the pin with a capacitor to GND to reduce noise pick-up. The voltage on the pin is top-limited by an internal zener. Activating the zener causes the IC to shut down (not latched). Tie the pin to RFmin if the function is not used.
8	DIS	Latched device shutdown. Internally the pin connects a comparator that, when the voltage on the pin exceeds 2V, shuts the IC down and brings its consumption almost to a "before start-up" level. The information is latched and it is necessary to recycle the supply voltage of the IC to enable it to restart: the latch is removed as the voltage on the Vcc pin goes below the UVLO threshold. Tie the pin to GND if the function is not used.

PIN FUNCTIONS (cont'd)

9	PFC_STOP	Open-drain ON/OFF control of PFC controller. This pin, normally open, is intended for stopping the PFC controller, for protection purpose or during burst-mode operation. It goes low when the IC is shut down by DIS>2 V, ISEN>1.5 V, LINE>6 V and STBY<1.25V. The pin is pulled low also when the voltage on pin DELAY exceeds 2V and goes back open as the voltage falls below 0.3V. During UVLO, it is open. Leave the pin unconnected if not used.
10	GND	Chip ground. Current return for both the low-side gate-drive current and the bias current of the IC. All of the ground connections of the bias components should be tied to a track going to this pin and kept separate from any pulsed current return.
11	LVG	Low-side gate-drive output. The driver is capable of 0.3 A min. source and 0.8 A min. sink peak current to drive the lower MOSFET of the half-bridge leg. The pin is actively pulled to GND during UVLO.
12	Vcc	Supply Voltage of both the signal part of the IC and the low-side gate driver. Sometimes a small bypass capacitor (0.1 µF typ.) to GND might be useful to get a clean bias voltage for the signal part of the IC.
13	N.C.	High-voltage spacer. The pin is not internally connected to isolate the high-voltage pin and ease compliance with safety regulations (creepage distance) on the PCB.
14	OUT	High-side gate-drive floating ground. Current return for the high-side gate-drive current. Layout carefully the connection of this pin to avoid too large spikes below ground.
15	HVG	High-side floating gate-drive output. The driver is capable of 0.3A min. source and 0.8A min. sink peak current to drive the upper MOSFET of the half-bridge leg. A resistor internally connected to pin 14 (OUT) ensures that the pin is not floating during UVLO.
16	VBOOT	High-side gate-drive floating supply Voltage. The bootstrap capacitor connected between this pin and pin 14 (OUT) is fed by an internal synchronous bootstrap diode driven in-phase with the low-side gate-drive. This patented structure replaces the normally used external diode.

TYPICAL SYSTEM BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Tj=0 to 105°C, Vcc=15V, V_{BOOT}=15V, C_{HVG}=C_{LVG}=1 nF; C_F=470 pF; R_{RFmin}=12 kΩ; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
IC SUPPLY VOLTAGE						
Vcc	Operating range	After device turn-on	8.7		16	V
Vcc_{On}	Turn-on threshold	Voltage rising	10	10.7	11.4	V
Vcc_{Off}	Turn-off threshold	Voltage falling	7.45	8.15	8.85	V
Hys	Hysteresis			2.55		V
V_Z	Vcc clamp voltage	Iclamp = 10 mA	16	17	17.5	V
SUPPLY CURRENT						
$I_{start-up}$	Start-up Current	Before device turn-on Vcc = Vcc_{On}- 0.2 V		200	250	µA
I_q	Quiescent Current	Device on, V_{STBY} = 1V		1.5	2	mA
I_{op}	Operating current			4		mA
I_q	Residual consumption	V_{DIS} > 2 V or V_{DELAY}>2V or V_{LINE}<1.25 V or V_{LINE}=V_{clamp}		300	400	µA
HIGH-SIDE FLOATING GATE-DRIVE SUPPLY						
I_{LKBOOT}	V_{BOOT} pin leakage current	V_{BOOT} = 580V			5	µA
I_{LKOUT}	OUT pin leakage current	V_{OUT} = 562V			5	µA
$R_{DS(on)}$	Synchronous bootstrap diode on-resistance	V_{LVG} = HIGH		150		Ω
OVERCURRENT COMPARATOR						
I_{ISEN}	Input Bias Current	V_{ISEN} = 0 to $V_{ISENdis}$			-1	µA
t_{LEB}	Leading Edge Blanking	After V_{HVG} and V_{LVG} low-to-high transition		250		ns
V_{ISENx}	Frequency shift threshold	Voltage rising (1)	0.76	0.8	0.84	V
	Hysteresis	Voltage falling		50		mV
$V_{ISENdis}$	Latch off threshold	Voltage rising (1)	1.44	1.5	1.56	V
$td_{(H-L)}$	Delay to Output				200	ns
LINE SENSING						
Vth	Threshold voltage	Voltage rising or falling (1)	1.2	1.25	1.3	V
I_{Hys}	Current Hysteresis	Vcc> 5V, V_{LINE} = 0.3V	12	15	18	µA
V_{clamp}	Clamp level	I_{LINE} = 1mA	6		8	V
DIS FUNCTION						
I_{DIS}	Input Bias Current	V_{DIS} = 0 to Vth			-1	µA
Vth	Disable threshold	Voltage rising (1) (2)	1.92	2	2.08	V
OSCILLATOR						
D	Output duty cycle	Both HVG and LVG	48	50	52	%
f_{osc}	Oscillation frequency		58.2	60	61.8	kHz
		R_{RFmin}= 3.48 kΩ	240	250	260	
T_D	Dead-time	Between HVG and LVG	0.2	0.27	0.35	µs
V_{CFp}	Peak value			3.9		V
V_{CFv}	Valley value			0.8		V
V_{REF}	Voltage reference at pin 4	(1)	1.92	2	2.08	V
K_M	Current mirroring ratio			1		A/A
PFC_STOP FUNCTION						
I_{leak}	High level leakage current	V_{PFC_STOP} =Vcc, V_{DIS} = 0 V			1	µA
V_L	Low saturation level	I_{PFC_STOP} =1mA, V_{DIS} =1.5 V			0.1	V

ELECTRICAL CHARACTERISTICS (cont'd)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SOFT-START FUNCTION						
I_{leak}	Open-state current	V(Css)= 2V			0.5	µA
R	Discharge resistance	$V_{ISEN}>V_{ISENx}$		100		Ω
STANDBY FUNCTION						
I_{DIS}	Input Bias Current	V_{DIS} = 0 to Vth			-1	µA
Vth	Disable threshold	Voltage falling (1)	1.2	1.25	1.3	V
Hys	Hysteresis	Voltage rising		50		mV
DELAYED SHUTDOWN FUNCTION						
I_{leak}	Open-state current	V(DELAY) = 0			0.5	µA
I_{CHARGE}	Charge current	V_{DELAY} = 1V, V_{ISEN}=0.85V	100	150	200	µA
T_{CHARGE}	Charge duration			20		µs
Vth_1	Threshold for forced operation at max. frequency	Voltage rising (1)	1.92	2	2.08	V
Vth_2	Shutdown threshold	Voltage rising (1)	3.3	3.5	3.7	V
Vth_3	Restart threshold	Voltage falling (1)	0.25	0.3	0.35	V
LOW-SIDE GATE DRIVER (voltages referred to GND)						
V_{LVGL}	Output Low Voltage	I_{sink} = 200 mA			1.5	V
V_{LVGH}	Output High voltage	I_{source} = 5 mA	12.8	13.3		V
$I_{sourcepk}$	Peak source current		-0.3			A
I_{sinkpk}	Peak sink current		0.8			A
t_f	Fall Time			30		ns
t_r	Rise Time			60		ns
	UVLO saturation	Vcc= 0 to Vcc_{On}, I_{sink}= 2mA			1.1	V
HIGH-SIDE GATE DRIVER (voltages referred to OUT)						
V_{LVGL}	Output Low Voltage	I_{sink} = 200 mA			1.5	V
V_{LVGH}	Output High voltage	I_{source} = 5 mA	12.8	13.3		V
$I_{sourcepk}$	Peak source current		-0.3			A
I_{sinkpk}	Peak sink current		0.8			A
t_f	Fall Time			30		ns
t_r	Rise Time			60		ns
	HVG-OUT pull-down			25		kΩ

(1) Values tracking each other

(2) This value will be reduced at 1.82V typ. in the final silicon release

PWM IC(IC7)：FAN7602M

FAIRCHILD SEMICONDUCTOR®

April 2006

FAN7602
Green Current Mode PWM Controller

Features

- Green Current Mode PWM Control
- Fixed 65kHz Operation with Frequency Modulation
- Internal High-Voltage Start-up Switch
- Burst Mode Operation
- Line Voltage Feed Forward to Limit Maximum Power
- Line Under-Voltage Protection
- Latch Protection & Internal Soft-Start (10ms) Function
- Overload Protection
- Over Voltage Protection
- Low Operation Current: Typ. 1mA
- 8-pin DIP

Applications

- Adapter
- LCD Monitor Power
- Auxiliary Power Supply

Related Application Notes

- **AN6014** - Green Current Mode PWM Controller FAN7602

Description

The FAN7602 is a green current mode PWM controller. It is specially designed for off-line adapter application, DVDP, VCR, LCD monitor application, and auxiliary power supplies.

The internal high-voltage start-up switch and the burst mode operation reduce the power loss in standby mode. Because of the internal start-up switch and the burst mode, it is possible to supply 0.5W load limiting the input power under 1W when the input line voltage is 265Vac. On no-load condition, the input power is under 0.3W.

The maximum power can be limited constantly, regardless of the line voltage change using the power limit function.

The switching frequency is internally fixed to be 65kHz and the frequency modulation technique reduces EMI.

The FAN7602 includes various protections for the system reliability and the internal soft start prevents the output voltage over-shoot at start-up.

Ordering Information

Part Number	Operating Temp. Range	Pb-Free	Package	Packing Method	Marking Code
FAN7602N	-25°C to +125°C	Yes	8-DIP	Rail	FAN7602

Typical Application Diagram

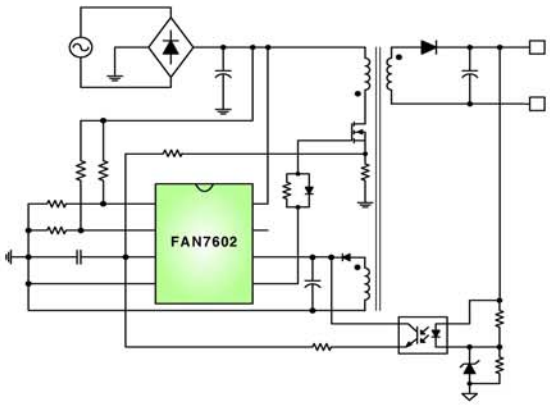


Figure 1. Typical Flyback Application

Internal Block Diagram

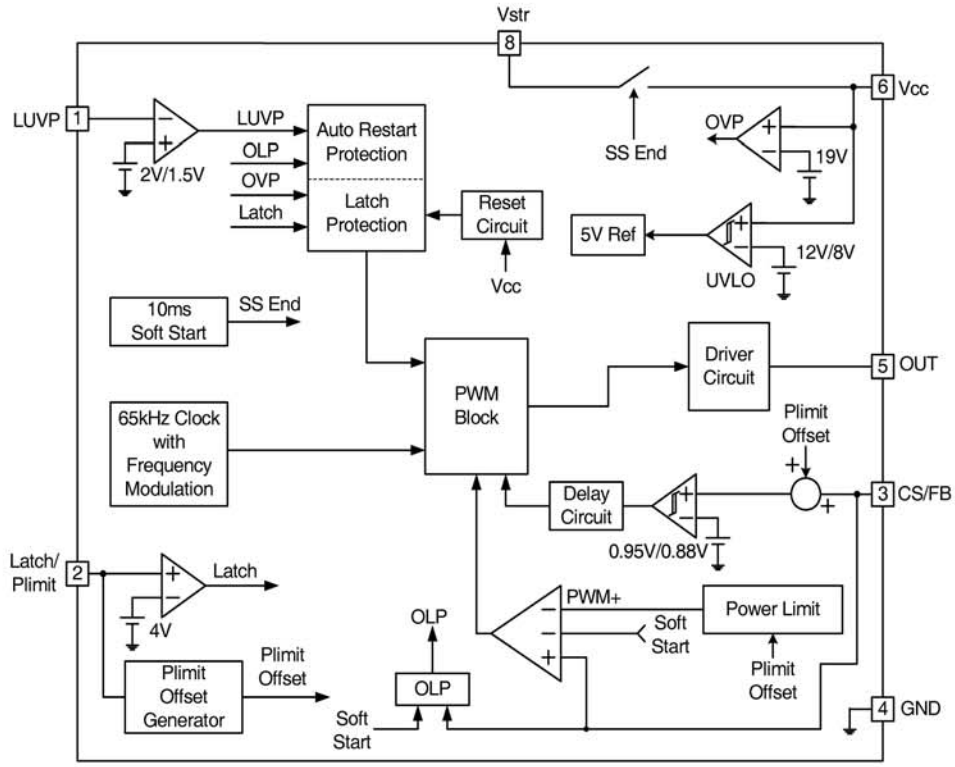


Figure 2. Functional Block Diagram of FAN7602

Pin Assignments

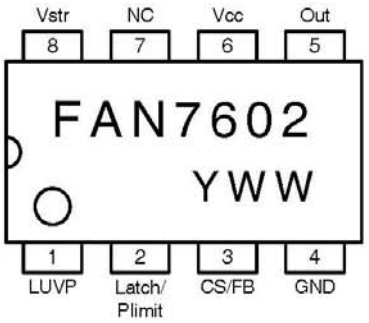


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	LUVP	**Line Under Voltage Protection Pin.** This pin is used to protect the set when the input voltage is lower than the rated input voltage range.
2	Latch/Plimit	**Latch Protection and Power Limit Pin.** When the pin voltage exceeds 4V, the latch protection works and the latch protection is reset when the Vcc voltage is lower than 5V. For the power limit function, the OCP level decreases as the pin voltage increases.
3	CS/FB	**Current Sense and Feedback Pin.** This pin is used to sense the MOSFET current for the current mode PWM and OCP. The output voltage feedback information and the current sense information are added using external RC filter.
4	GND	**Ground Pin.** This pin is used for the ground potential of all the pins. For proper operation, the signal ground and the power ground should be separated.
5	OUT	**Gate Drive Output Pin.** This pin is an output pin to drive an external MOSFET. The peak sourcing current is 450mA and the peak sinking current is 600mA. For proper operation, the stray inductance in the gate driving path must be minimized.
6	Vcc	**Supply Voltage Pin.** IC operating current and MOSFET driving current are supplied using this pin.
7	NC	**No Connection.**
8	Vstr	**Start-up Pin.** This pin is used to supply IC operating current during IC start-up. After start-up, the internal JFET is turned off to reduce power loss.

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table defines the conditions for actual device operation.

Symbol	Parameter	Value	Unit
Vcc	Supply Voltage	20	V
I_{OH}, I_{OL}	Peak Drive Output Current	+450/-600	mA
$V_{CS/FB}$	CS/FB Input Voltage	-0.3 to 20	V
V_{LUVP}	LUVP Input Voltage	-0.3 to 10	V
V_{Latch}	Latch/Plimit Input Voltage	-0.3 to 10	V
Vstr	Vstr Input Voltage	600	V
Tj	Operating Junction Temperature	150	°C
Topr	Operating Temperature Range	-25 to 125	°C
Tstg	Storage Temperature Range	-55 to 150	°C
P_D	Power Dissipation	1.2	W
V_{ESD_HBM}	ESD Capability, Human Body Model	2.0	kV
V_{ESD_MM}	ESD Capability, Machine Model	300	V
V_{ESD_CDM}	ESD Capability, Charged Device Model	500	V

Thermal Impedance

Symbol	Parameter		Value	Unit
Rθja	Thermal Resistance, Junction to Ambient	8-DIP	100	°C/W

Note:

1. Regarding the test environment and PCB type, please refer to JESD51-2 and JESD51-10.

Electrical Characteristics

(Vcc = 14V, T_A = -25°C~125°C, unless otherwise specified)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
START UP SECTION						
I_{str}	Vstr Start-up Current	V_{str} = 30V, T_A = 25°C	0.7	1	1.4	mA
UNDER VOLTAGE LOCK OUT SECTION						
Vth(start)	Start Threshold Voltage	Vcc increasing	11	12	13	V
Vth(stop)	Stop Threshold Voltage	Vcc decreasing	7	8	9	V
HY(uvlo)	UVLO Hysteresis		3.6	4	4.4	V
SUPPLY CURRENT SECTION						
Ist	Start-up Supply Current	T_A = 25°C	-	250	320	µA
Icc	Operating Supply Current	Output no switching	-	1	1.5	mA
SOFT START SECTION						
Tss	Soft Start Time(1)		5	10	15	ms
PWM SECTION						
F_{OSC}	Operating Frequency	$V_{CS/FB}$ = 0.2V, T_A = 25°C	59	65	73	kHz
ΔF	Frequency Modulation		-	±2	-	kHz
$V_{CS/FB1}$	CS/FB Threshold Voltage	T_A = 25°C	0.9	1.0	1.1	V
T_D	Propagation Delay to Output(1)		-	100	150	ns
D_{MAX}	Maximum Duty Cycle		70	75	80	%
D_{MIN}	Minimum Duty Cycle		-	-	0	%
BURST MODE SECTION						
$V_{CS/FB2}$	Burst On Threshold Voltage	T_A = 25°C	0.84	0.95	1.06	V
$V_{CS/FB3}$	Burst Off Threshold Voltage	T_A = 25°C	0.77	0.88	0.99	V
POWER LIMIT SECTION						
K_{Plimit}	Offset Gain	$V_{Latch/Plimit}$ = 2V, T_A = 25°C	0.12	0.16	0.20	
OUTPUT SECTION						
V_{OH}	Output Voltage High	T_A = 25°C, Isource = 100mA	11.5	12	14	V
V_{OL}	Output Voltage Low	T_A = 25°C, Isink = 100mA	-	1	2.5	V
Tr	Rising Time(1)	T_A = 25°C, Cl = 1nF	-	45	150	ns
Tf	Falling Time(1)	T_A = 25°C, Cl = 1nF	-	35	150	ns

Note:

1. These parameters, although guaranteed by design, are not tested in mass production.

Electrical Characteristics (Continued)

(Vcc = 14V, T_A = -25°C~125°C, unless otherwise specified)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
PROTECTION SECTION						
V_{Latch}	Latch Voltage		3.6	4	4.4	V
T_{OLP}	Overload Protection Time (1)		20	22	24	ms
T_{OLP_ST}	Overload Protection Time at Start-up		30	37	44	ms
V_{OLP}	Overload Protection Level		-	0	0.1	V
$V_{LUVPoff}$	Line Under-Voltage Protection On to Off	T_A = 25°C	1.9	2	2.1	V
V_{LUVPon}	Line Under-Voltage Protection Off to On	T_A = 25°C	1.4	1.5	1.6	V
V_{OVP}	Over Voltage Protection	T_A = 25°C	18	19	20	V

Note:

1. These parameters, although guaranteed by design, are not tested in mass production.

Applications Information

1. Start-up Circuit and Soft Start Block

The FAN7602 contains a start-up switch to reduce the power loss of the external start-up circuit of the conventional PWM converters. The internal start-up circuit charges the Vcc capacitor with 0.9mA current source if the AC line is connected. The start-up switch is turned off 15ms after IC starts up, as shown in Fig. 19. The soft-start function starts when the Vcc voltage reaches the start threshold voltage of 12V and ends when the internal soft-start voltage reaches 1V. The internal start-up circuit starts charging the Vcc capacitor again if the Vcc voltage is lowered to the minimum operating voltage, 8V. The UVLO block shuts down the output drive circuit and some blocks to reduce the IC operating current and the internal soft-start voltage drops to zero. If the Vcc voltage reaches the start threshold voltage, the IC starts switching again and the soft start block works as well.

During the soft start, pulse-width modulated (PWM) comparator compares the CS/FB pin voltage with the soft start voltage. The soft-start voltage starts from 0.5V and the soft-start ends when it reaches 1V and the soft-start time is 10ms. The start-up switch is turned off when the soft start voltage reaches 1.5V.

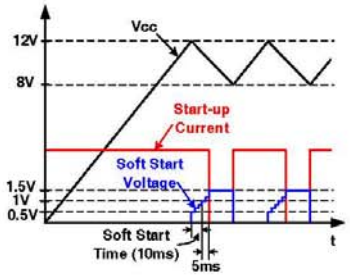


Figure 19. Start-up Current and Vcc Voltage

2. Oscillator Block

The oscillator frequency is set internally and a frequency modulation (FM) function reduces EMI. The average frequency is 65kHz and the modulation frequency is ±2kHz. The frequency varies from 63kHz to 67kHz with 16 steps. The frequency step is 250Hz and FM frequency is 125Hz, as shown in Fig. 20.

3. Current Sense and Feedback Block

The FAN7602 performs the current sensing for the current mode PWM and the output voltage feedback with only one pin, pin3. To achieve the two functions with one pin, an internal LEB (leading edge blanking) circuit to filter the current sense noise is not included because the external RC filter is necessary to add the output voltage feedback information and the current sense information. Fig. 21 shows the current sense and feedback circuits. R_S is the current sense resistor to sense the switch current. The current sense information is filtered by an RC filter composed of R_F and C_F. According to the output voltage feedback information, I_{FB} charges or stops charging C_F to adjust the offset voltage. If I_{FB} is zero, C_F is discharged through R_F and R_S to lower the offset voltage.

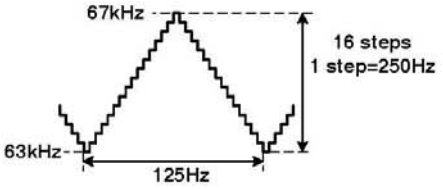


Figure 20. Frequency Modulation

Figure 22 shows typical voltage waveforms of the CS/FB pin. The current sense waveform is added to the offset voltage as shown in the figure. The CS/FB pin voltage is compared with PWM+ that is 1V - Plimit offset as shown in Fig. 22. If the CS/FB voltage meets PWM+, the output drive is shut off. As shown in Fig. 22, if the feedback offset voltage is low, the switch on time is increased. If the feedback offset voltage is high, then the switch on time is decreased. In this way, the duty cycle is controlled according to the output load condition. In general, the maximum output power increases as the input voltage increases because the current slope during switch on-time increases. To limit the output power of the converter constantly, the power limit function is included in the FAN7602. Sensing the converter input voltage through the Latch/Plimit pin, the Plimit offset voltage is subtracted from 1V. As shown in Fig. 22, the Plimit offset voltage is subtracted from 1V and the switch on-time decreases as the Plimit offset voltage increases. If the converter input voltage increases, the switch on-time decreases, controlling the output power constant. The offset voltage is proportional to the Latch/Plimit pin voltage and the gain is 0.16; if the Latch/Plimit voltage is 1V, the offset voltage is 0.16V.

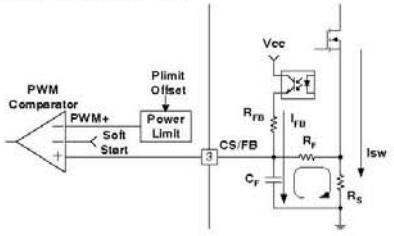


Figure 21. Current Sense and Feedback Circuits

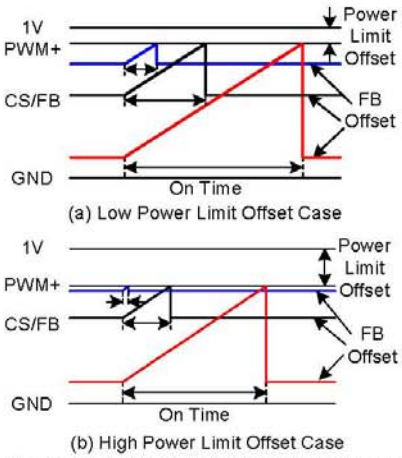


Figure 22. CS/FB Pin Voltage Waveforms

4. Burst Mode Block

The FAN7602 contains the burst mode block to reduce the power loss at a light load and no load as the FAN7601. A hysteresis comparator senses the offset voltage of the Burst+ for the burst mode as shown in Fig. 23. The Burst+ is the sum of the CS/FB voltage and Plimit offset voltage. The FAN7602 enters the burst mode when the offset voltage of the Burst+ is higher than 0.95V and exits the burst mode when the offset voltage is lower than 0.88V. The offset voltage is sensed during the switch off time.

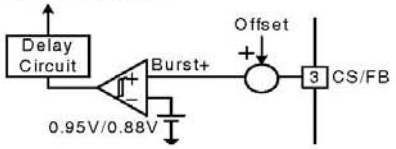


Figure 23. Burst Mode Block

5. Protection Block

The FAN7602 contains several protection functions to improve system reliability.

5.1 Overload Protection (OLP)

The FAN7602 contains the overload protection function. If the output load is higher than the rated output current, the output voltage drops and the feedback error amplifier is saturated. The offset of the CS/FB voltage representing the feedback information is almost zero. As shown in Fig. 24, the CS/FB voltage is compared with 50mV reference when the internal clock signal is high and, if the voltage is lower than 50mV, the OLP timer starts counting. If the OLP condition persists for 22ms, the timer generates the OLP signal. And this protection is reset by the UVLO. The OLP block is enabled after the soft start finishes.

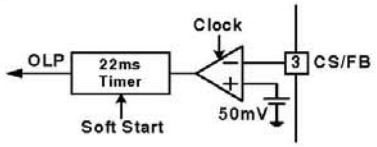


Figure 24. Overload Protection Circuit

5.2 Line Under Voltage Protection

If the input voltage of the converter is lower than the minimum operating voltage, the converter input current increases too much, causing component failure. Therefore, if the input voltage is low, the converter should be protected. In the FAN7602, the LUVP circuit senses the input voltage using the LUVP pin and, if this voltage is lower than 2V, the LUVP signal is generated. The comparator has 0.5V hysteresis. If the LUVP signal is generated, the output drive block is shut down, the output voltage feedback loop is saturated, and the OLP works if the LUVP condition persists more than 22ms.

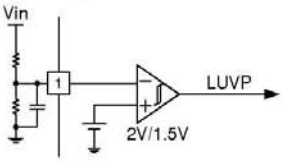


Figure 25. Line UVP Circuit

5.3 Latch Protection

The latch protection is provided to protect the system against abnormal conditions using the Latch/Plimit pin. The Latch/Plimit pin can be used for the output overvoltage protection and/or other protections. If the Latch/Plimit pin voltage is made higher than 4V by an external circuit, the IC is shut down. The latch protection is reset when the Vcc voltage is lower than 5V.

5.4 Over-Voltage Protection (OVP)

If the Vcc voltage reaches 19V, the IC shuts down and the OVP protection is reset when the Vcc voltage is lower than 5V.

6. Output Drive Block

The FAN7602 contains a single totem-pole output stage to drive a power MOSFET. The drive output is capable of up to 450mA sourcing current and 600mA sinking current with typical rise and fall time of 45ns, 35ns respectively with a 1nF load.

PFC IC(IC4)：L6562D

L6562

TRANSITION-MODE PFC CONTROLLER

1 Features

- REALISED IN BCD TECHNOLOGY
- TRANSITION-MODE CONTROL OF PFC PRE-REGULATORS
- PROPRIETARY MULTIPLIER DESIGN FOR MINIMUM THD OF AC INPUT CURRENT
- VERY PRECISE ADJUSTABLE OUTPUT OVERVOLTAGE PROTECTION
- ULTRA-LOW (≤70µA) START-UP CURRENT
- LOW (≤4 mA) QUIESCENT CURRENT
- EXTENDED IC SUPPLY VOLTAGE RANGE
- ON-CHIP FILTER ON CURRENT SENSE
- DISABLE FUNCTION
- 1% (@ Tj = 25 °C) INTERNAL REFERENCE VOLTAGE
- -600/+800mA TOTEM POLE GATE DRIVER WITH UVLO PULL-DOWN AND VOLTAGE CLAMP
- DIP-8/SO-8 PACKAGES ECOPACK®

1.1 APPLICATIONS

- PFC PRE-REGULATORS FOR:
  - IEC61000-3-2 COMPLIANT SMPS (TV, DESKTOP PC, MONITOR) UP TO 300W
  - HI-END AC-DC ADAPTER/CHARGER
  - ENTRY LEVEL SERVER & WEB SERVER

Figure 1. Packages


DIP-8


SO-8

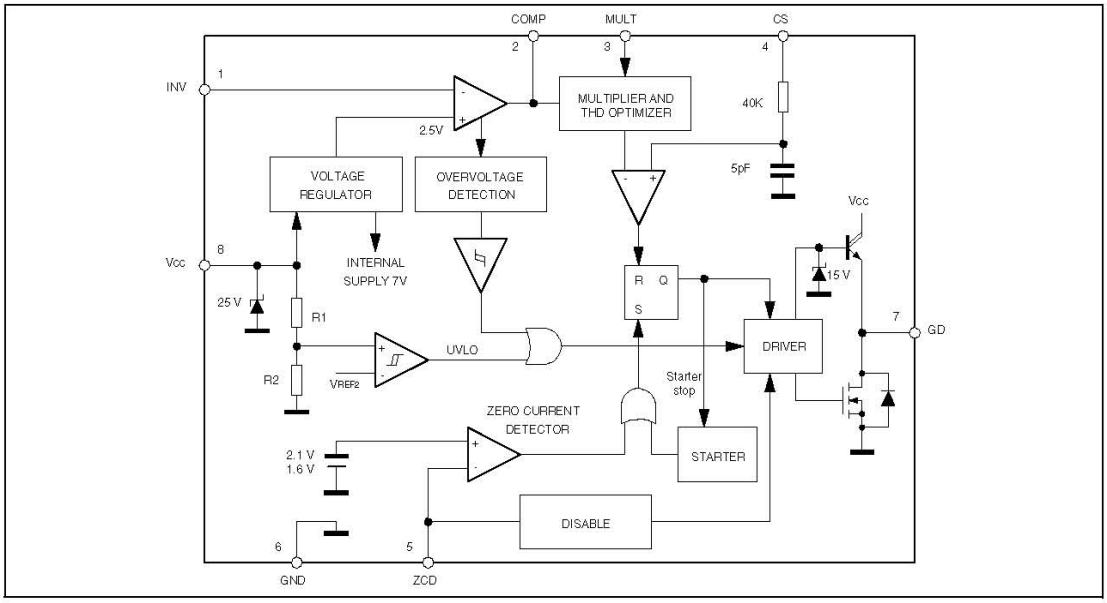
Table 1. Order Codes

Part Number	Package
L6562N	DIP-8
L6562D	SO-8
L6562DTR	Tape & Reel

2 Description

The L6562 is a current-mode PFC controller operating in Transition Mode (TM). Pin-to-pin compatible with the predecessor L6561, it offers improved performance.

Figure 2. Block Diagram



2 Description (continued)

The highly linear multiplier includes a special circuit, able to reduce AC input current distortion, that allows wide-range-mains operation with an extremely low THD, even over a large load range.

The output voltage is controlled by means of a voltage-mode error amplifier and a precise (1% @Tj = 25°C) internal voltage reference.

The device features extremely low consumption (≤70 µA before start-up and <4 mA running) and includes a disable function suitable for IC remote ON/OFF, which makes it easier to comply with energy saving norms (Blue Angel, EnergyStar, Energy2000, etc.).

An effective two-step OVP enables to safely handle overvoltages either occurring at start-up or resulting from load disconnection.

The totem-pole output stage, capable of 600 mA source and 800 mA sink current, is suitable for big MOS-FET or IGBT drive which, combined with the other features, makes the device an excellent low-cost solution for EN61000-3-2 compliant SMPS's up to 300W.

Table 2. Absolute Maximum Ratings

Symbol	Pin	Parameter	Value	Unit
V_{CC}	8	IC Supply voltage (Icc = 20 mA)	self-limited	V
---	1 to 4	Analog Inputs & Outputs	-0.3 to 8	V
IZCD	5	Zero Current Detector Max. Current	-50 (source) 10 (sink)	mA
P_{tot}		Power Dissipation @Tamb = 50°C (DIP-8) (SO-8)	1 0.65	W
T_j		Junction Temperature Operating range	-40 to 150	°C
T_{stg}		Storage Temperature	-55 to 150	°C

Figure 3. Pin Connection (Top view)

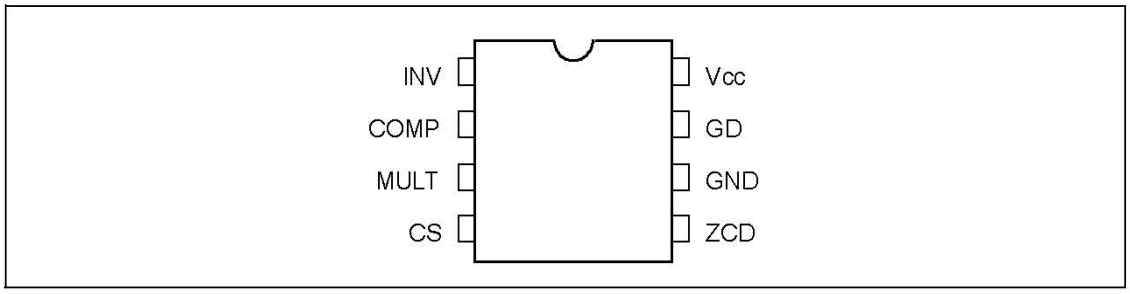


Table 3. Thermal Data

Symbol	Parameter	SO8	Minidip	Unit
$R_{th\ j\text{-}amb}$	Max. Thermal Resistance, Junction-to-ambient	150	100	°C/W

Table 4. Pin Description

N°	Pin	Function
1	INV	Inverting input of the error amplifier. The information on the output voltage of the PFC pre-regulator is fed into the pin through a resistor divider.
2	COMP	Output of the error amplifier. A compensation network is placed between this pin and INV (pin #1) to achieve stability of the voltage control loop and ensure high power factor and low THD.
3	MULT	Main input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop.
4	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal sinusoidal-shaped reference, generated by the multiplier, to determine MOSFET's turn-off.
5	ZCD	Boost inductor's demagnetization sensing input for transition-mode operation. A negative-going edge triggers MOSFET's turn-on.
6	GND	Ground. Current return for both the signal part of the IC and the gate driver.
7	GD	Gate driver output. The totem pole output stage is able to drive power MOSFET's and IGBT's with a peak current of 600 mA source and 800 mA sink. The high-level voltage of this pin is clamped at about 12V to avoid excessive gate voltages in case the pin is supplied with a high Vcc.
8	Vcc	Supply Voltage of both the signal part of the IC and the gate driver. The supply voltage upper limit is extended to 22V min. to provide more headroom for supply voltage changes.

Table 5. Electrical Characteristics

(T_j = -25 to 125°C, V_{CC} = 12, C_O = 1 nF; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE						
V_{CC}	Operating range	After turn-on	10.3		22	V
V_{CCon}	Turn-on threshold	(1)	11	12	13	V
V_{CCOff}	Turn-off threshold	(1)	8.7	9.5	10.3	V
Hys	Hysteresis		2.2		2.8	V
V_Z	Zener Voltage	I_{CC} = 20 mA	22	25	28	V
SUPPLY CURRENT						
$I_{start-up}$	Start-up Current	Before turn-on, V_{CC} =11V		40	70	µA
I_q	Quiescent Current	After turn-on		2.5	3.75	mA
I_{CC}	Operating Supply Current	@ 70 kHz		3.5	5	mA
I_q	Quiescent Current	During OVP (either static or dynamic) or V_{ZCD} =150 mV			2.2	mA
MULTIPLIER INPUT						
I_{MULT}	Input Bias Current	V_{VFF} = 0 to 4 V			-1	µA
V_{MULT}	Linear Operation Range		0 to 3			V
$\frac{\Delta V_{CS}}{\Delta V_{MULT}}$	Output Max. Slope	V_{MULT} = 0 to 0.5V V_{COMP} = Upper clamp	1.65	1.9		V/V
K	Gain (2)	V_{MULT} = 1 V, V_{COMP} = 4 V	0.5	0.6	0.7	1/V
ERROR AMPLIFIER						
V_{INV}	Voltage Feedback Input Threshold	T_j = 25 °C	2.465	2.5	2.535	V
		10.3 V < Vcc < 22 V (1)	2.44		2.56	
	Line Regulation	Vcc = 10.3 V to 22V		2	5	mV
I_{INV}	Input Bias Current	V_{INV} = 0 to 3 V			-1	µA

Table 5. Electrical Characteristics (continued)
(T_j = -25 to 125°C, V_{CC} = 12, C_O = 1 nF; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_v	Voltage Gain	Open loop	60	80		dB
GB	Gain-Bandwidth Product			1		MHz
I_{COMP}	Source Current	V_{COMP} = 4V, V_{INV} = 2.4 V	-2	-3.5	-5	mA
	Sink Current	V_{COMP} = 4V, V_{INV} = 2.6 V	2.5	4.5		mA
V_{COMP}	Upper Clamp Voltage	I_{SOURCE} = 0.5 mA	5.3	5.7	6	V
	Lower Clamp Voltage	I_{SINK} = 0.5 mA (1)	2.1	2.25	2.4	V
CURRENT SENSE COMPARATOR						
I_{CS}	Input Bias Current	V_{CS} = 0			-1	µA
$t_{d(H-L)}$	Delay to Output			200	350	ns
$V_{CS\ clamp}$	Current sense reference clamp	V_{COMP} = Upper clamp	1.6	1.7	1.8	V
$V_{CSoffset}$	Current sense offset	V_{MULT} = 0		30		mV
		V_{MULT} = 2.5V		5		
ZERO CURRENT DETECTOR						
V_{ZCDH}	Upper Clamp Voltage	I_{ZCD} = 2.5 mA	5.0	5.7	6.5	V
V_{ZCDL}	Lower Clamp Voltage	I_{ZCD} = -2.5 mA	0.3	0.65	1	V
V_{ZCDA}	Arming Voltage (positive-going edge)	(3)		2.1		V
V_{ZCDT}	Triggering Voltage (negative-going edge)	(3)		1.6		V
I_{ZCDb}	Input Bias Current	V_{ZCD} = 1 to 4.5 V		2		µA
I_{ZCDsrc}	Source Current Capability		-2.5		-5.5	mA
I_{ZCDsnk}	Sink Current Capability		2.5			mA
V_{ZCDdis}	Disable threshold		150	200	250	mV
V_{ZCDen}	Restart threshold				350	mV
I_{ZCDres}	Restart Current after Disable		30	75		µA
STARTER						
t_{START}	Start Timer period		75	130	300	µs
OUTPUT OVERVOLTAGE						
I_{OVP}	Dynamic OVP triggering current		35	40	45	µA
Hys	Hysteresis	(3)		30		µA
	Static OVP threshold	(1)	2.1	2.25	2.4	V
GATE DRIVER						
V_{OH}	Dropout Voltage	$I_{GDsource}$ = 20 mA		2	2.6	
		$I_{GDsource}$ = 200 mA		2.5	3	V
V_{OL}		I_{GDsink} = 200 mA		0.9	1.9	V
t_f	Voltage Fall Time			30	70	ns
t_r	Voltage Rise Time			40	80	ns
V_{Oclamp}	Output clamp voltage	$I_{GDsource}$ = 5mA; Vcc = 20V	10	12	15	V
	UVLO saturation	V_{CC} = 0 to V_{CCon}, I_{sink}=10mA			1.1	V

(1) All parameters are in tracking
(2) The multiplier output is given by: $V_{cs} = K \cdot V_{MULT} \cdot (V_{COMP} - 2.5)$
(3) Parameters guaranteed by design, functionality tested in production.

Figure 20. Gate-drive clamp vs. T_j

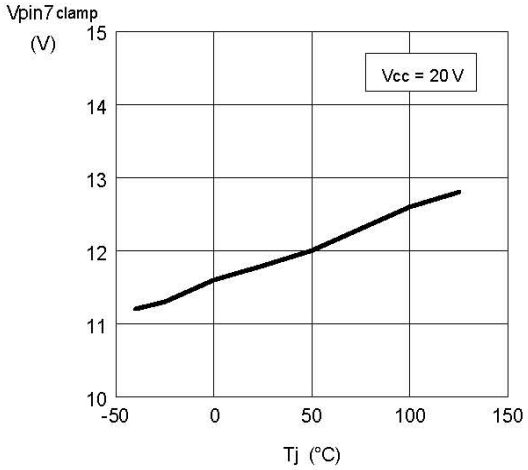
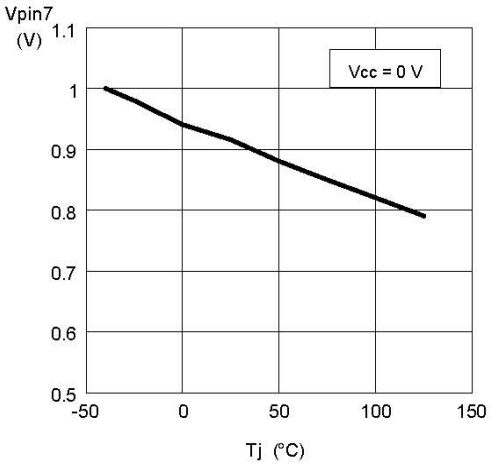


Figure 21. UVLO saturation vs. T_j



4 Application Information

4.1 Overvoltage protection

Under steady-state conditions, the voltage control loop keeps the output voltage Vo of a PFC pre-regulator close to its nominal value, set by the resistors R1 and R2 of the output divider. Neglecting ripple components, the current through R1, I_{R1}, equals that through R2, I_{R2}. Considering that the non-inverting input of the error amplifier is internally referenced at 2.5V, also the voltage at pin INV will be 2.5V, then:

$$I_{R2} = \frac{2.5}{R2} = I_{R1} = \frac{Vo - 2.5}{R1} \quad .$$

If the output voltage experiences an abrupt change $\Delta Vo > 0$ due to a load drop, the voltage at pin INV will be kept at 2.5V by the local feedback of the error amplifier, a network connected between pins INV and COMP that introduces a long time constant to achieve high PF (this is why ΔVo can be large). As a result, the current through R2 will remain equal to 2.5/R2 but that through R1 will become:

$$I'_{R1} = \frac{Vo - 2.5 + \Delta Vo}{R1} \quad .$$

The difference current $\Delta I_{R1}=I'_{R1}-I_{R2}=I'_{R1}-I_{R1}=\Delta Vo/R1$ will flow through the compensation network and enter the error amplifier output (pin COMP). This current is monitored inside the L6562 and if it reaches about 37 µA the output voltage of the multiplier is forced to decrease, thus smoothly reducing the energy delivered to the output. As the current exceeds 40 µA, the OVP is triggered (Dynamic OVP): the gate-drive is forced low to switch off the external power transistor and the IC put in an idle state. This condition is maintained until the current falls below approximately 10 µA, which re-enables the internal starter and allows switching to restart. The output ΔVo that is able to trigger the Dynamic OVP function is then:

$$\Delta Vo = R1 \cdot 40 \cdot 10^{-6} \quad .$$

An important advantage of this technique is that the OV level can be set independently of the regulated output voltage: the latter depends on the ratio of R1 to R2, the former on the individual value of R1. Another advantage is the precision: the tolerance of the detection current is 12%, that is 12% tolerance on ΔVo. Since $\Delta Vo << Vo$, the tolerance on the absolute value will be proportionally reduced.

Example: Vo = 400 V, ΔVo = 40 V. Then: R1=40V/40µA=1MΩ; R2=1MΩ·2.5/(400-2.5)=6.289kΩ. The tolerance on the OVP level due to the L6562 will be 40·0.12=4.8V, that is 1.2% of the regulated value.

When the load of a PFC pre-regulator is very low, the output voltage tends to stay steadily above the nominal value, which cannot be handled by the Dynamic OVP. If this occurs, however, the error amplifier output will saturate low; hence, when this is detected, the external power transistor is switched off and the IC put in an idle state (Static OVP). Normal operation is resumed as the error amplifier goes back into its linear region. As a result, the L6562 will work in burst-mode, with a repetition rate that can be very low.

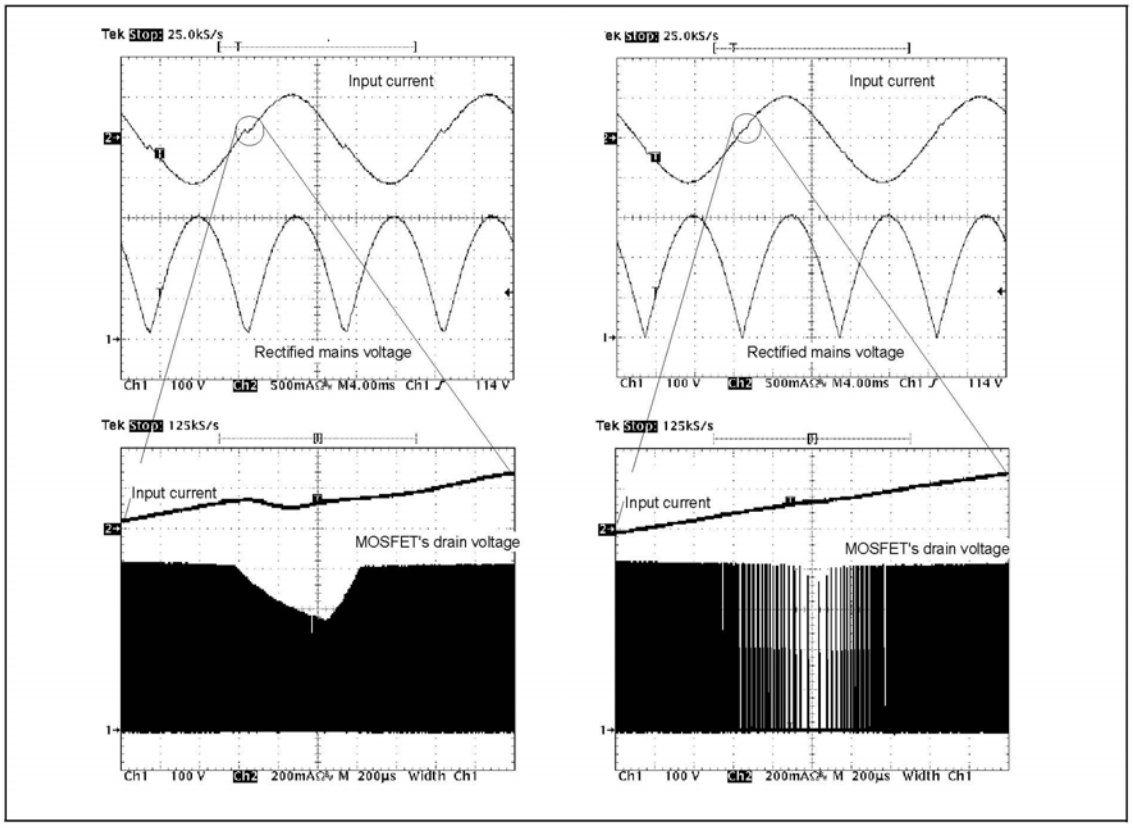
When either OVP is activated the quiescent consumption of the IC is reduced to minimize the discharge of the Vcc capacitor and increase the hold-up capability of the IC supply system.

4.2 THD optimizer circuit

The L6562 is equipped with a special circuit that reduces the conduction dead-angle occurring to the AC input current near the zero-crossings of the line voltage (crossover distortion). In this way the THD (Total Harmonic Distortion) of the current is considerably reduced.

A major cause of this distortion is the inability of the system to transfer energy effectively when the instantaneous line voltage is very low. This effect is magnified by the high-frequency filter capacitor placed after the bridge rectifier, which retains some residual voltage that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop.

Figure 22. THD optimization: standard TM PFC controller (left side) and L6562 (right side)



To overcome this issue the circuit embedded in the L6562 forces the PFC pre-regulator to process more energy near the line voltage zero-crossings as compared to that commanded by the control loop. This will result in both minimizing the time interval where energy transfer is lacking and fully discharging the high-frequency filter capacitor after the bridge. The effect of the circuit is shown in figure 23, where the key waveforms of a standard TM PFC controller are compared to those of the L6562.

Essentially, the circuit artificially increases the ON-time of the power switch with a positive offset added to

the output of the multiplier in the proximity of the line voltage zero-crossings. This offset is reduced as the instantaneous line voltage increases, so that it becomes negligible as the line voltage moves toward the top of the sinusoid.

To maximally benefit from the THD optimizer circuit, the high-frequency filter capacitor after the bridge rectifier should be minimized, compatibly with EMI filtering needs. A large capacitance, in fact, introduces a conduction dead-angle of the AC input current in itself - even with an ideal energy transfer by the PFC pre-regulator - thus making the action of the optimizer circuit little effective.

Figure 23. Typical application circuit (250W, Wide-range mains)

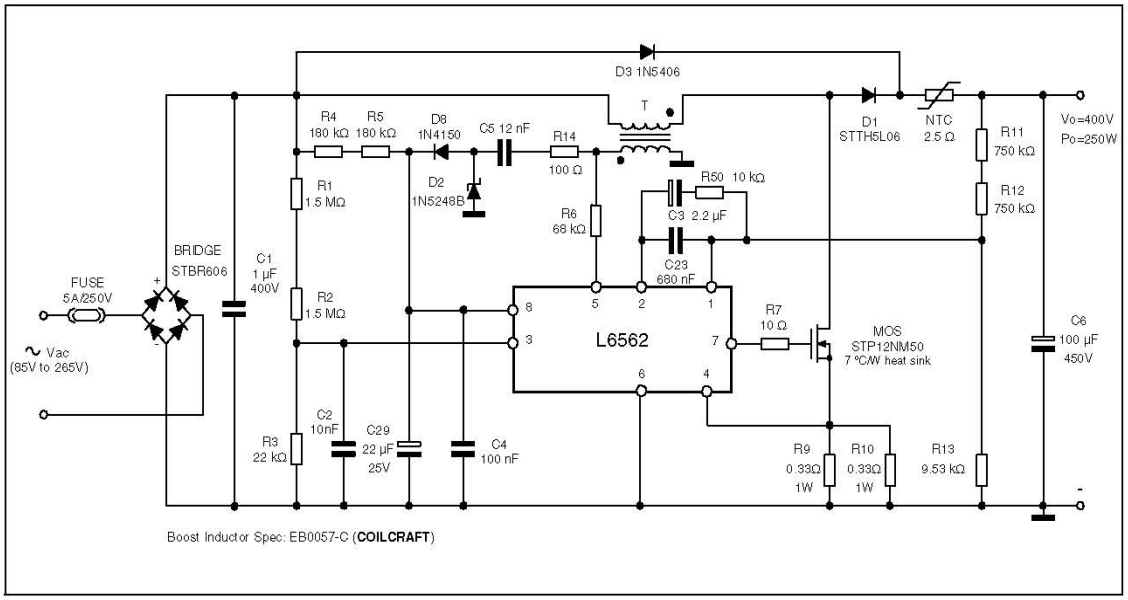
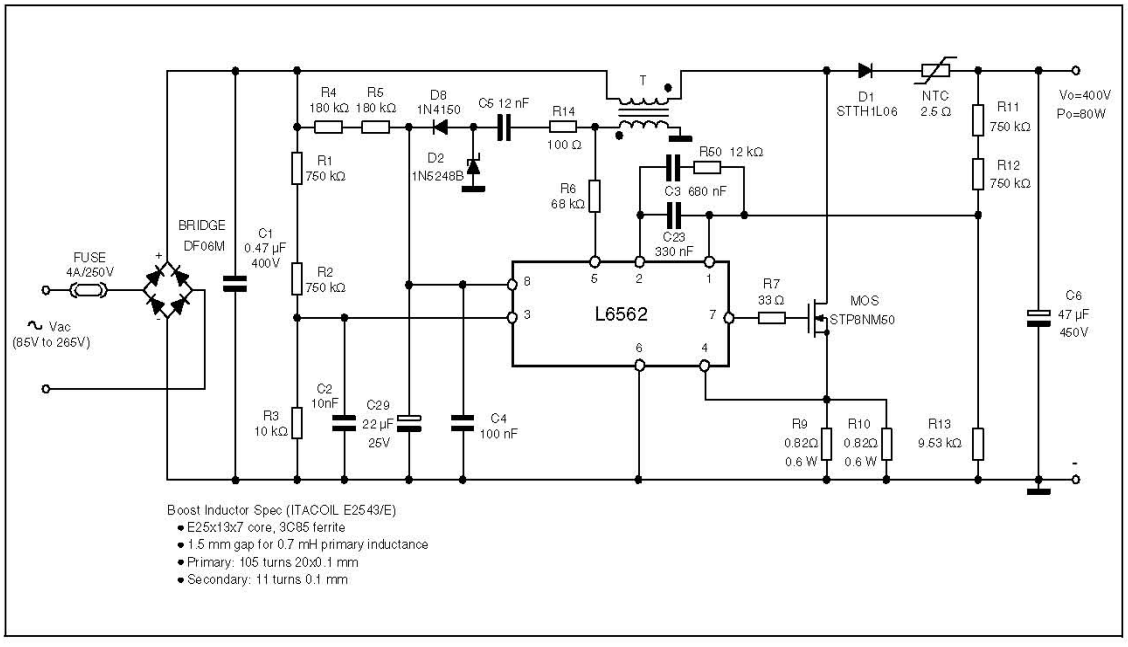


Figure 24. Demo board (EVAL6562-80W, Wide-range mains): Electrical schematic



PROTECTION CIRCUIT IC(ICS2)：LM393

LM393, LM293, LM2903, LM2903V, NCV2903

Low Offset Voltage Dual Comparators

The LM393 series are dual independent precision voltage comparators capable of single or split supply operation. These devices are designed to permit a common mode range−to−ground level with single supply operation. Input offset voltage specifications as low as 2.0 mV make this device an excellent selection for many applications in consumer, automotive, and industrial electronics.

Features

- Wide Single−Supply Range: 2.0 Vdc to 36 Vdc
- Split−Supply Range: ±1.0 Vdc to ±18 Vdc
- Very Low Current Drain Independent of Supply Voltage: 0.4 mA
- Low Input Bias Current: 25 nA
- Low Input Offset Current: 5.0 nA
- Low Input Offset Voltage: 5.0 mV (max) LM293/393
- Input Common Mode Range to Ground Level
- Differential Input Voltage Range Equal to Power Supply Voltage
- Output Voltage Compatible with DTL, ECL, TTL, MOS, and CMOS Logic Levels
- ESD Clamps on the Inputs Increase the Ruggedness of the Device without Affecting Performance
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes
- Pb−Free Packages are Available

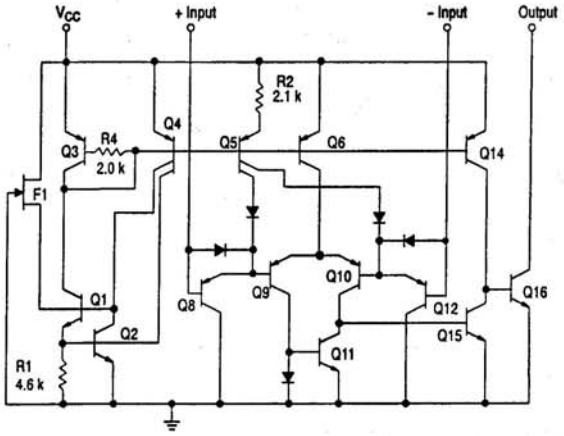


Figure 1. Representative Schematic Diagram
(Diagram shown is for 1 comparator)

ON Semiconductor®

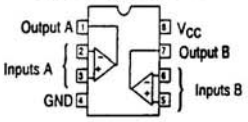
http://onsemi.com

PDIP−8
N SUFFIX
CASE 626

SOIC−8
D SUFFIX
CASE 751

Micro8™
DM SUFFIX
CASE 846A

PIN CONNECTIONS



(Top View)

DEVICE MARKING & ORDERING INFORMATION

See detailed ordering and shipping information and marking information in the package dimensions section on pages 6 and 7 of this data sheet.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+36 or ±18	Vdc
Input Differential Voltage Range	V_{IDR}	36	Vdc
Input Common Mode Voltage Range	V_{ICR}	−0.3 to +36	Vdc
Output Short Circuit−to−Ground Output Sink Current (Note 1)	I_{SC} I_{Sink}	Continuous 20	mA
Power Dissipation @ T_A = 25°C Derate above 25°C	P_D $1/R_{\theta JA}$	570 5.7	mW mW/°C
Operating Ambient Temperature Range LM293 LM393 LM2903 LM2903V, NCV2903 (Note 2)	T_A	 −25 to +85 0 to +70 −40 to +105 −40 to +125	°C
Maximum Operating Junction Temperature LM393, 2903, LM2903V LM293, NCV2903	$T_{J(max)}$	 150 150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
ESD Protection at any Pin − Human Body Model − Machine Model	V_{esd}	 2000 200	V

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}, output short circuits to V_{CC} can cause excessive heating and eventual destruction.
2. *NCV2903 is qualified for automotive use.*

MAXIMUM RATINGS

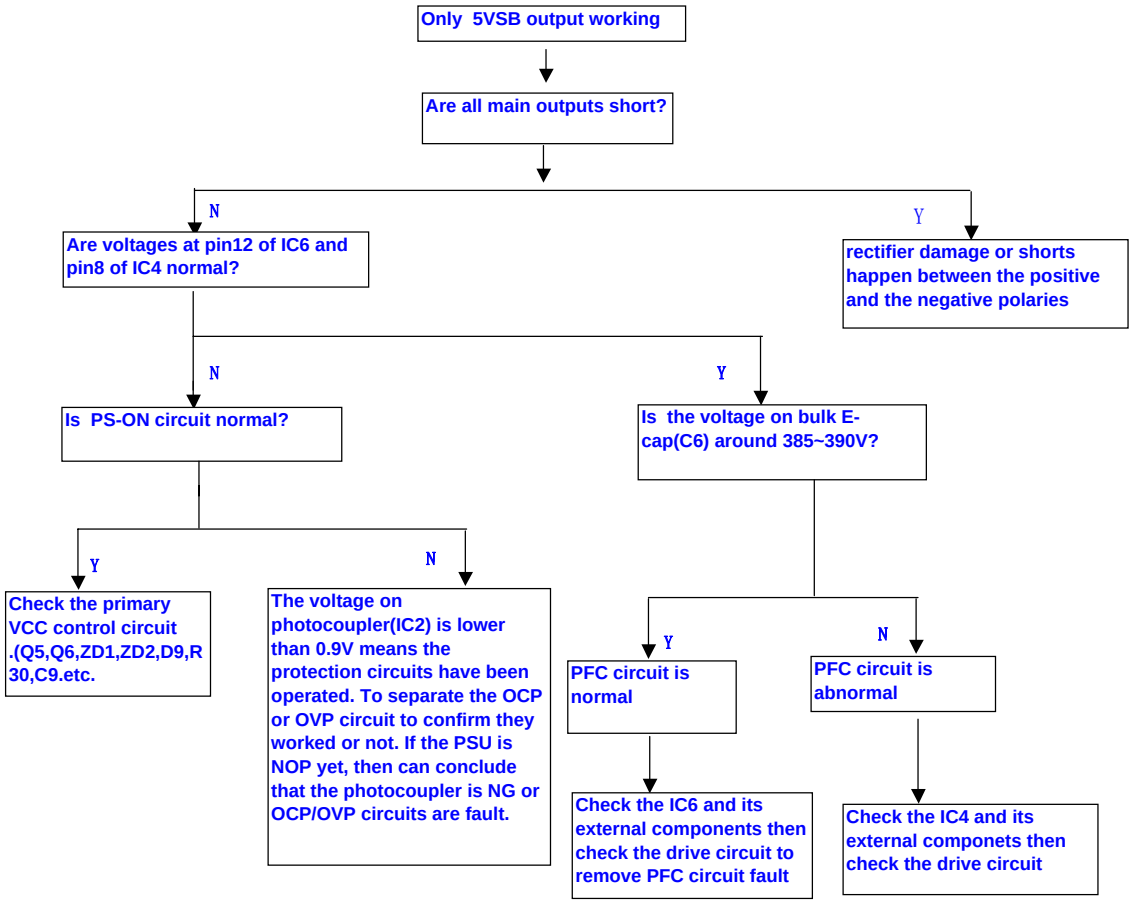
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+36 or ±18	Vdc
Input Differential Voltage Range	V_{IDR}	36	Vdc
Input Common Mode Voltage Range	V_{ICR}	−0.3 to +36	Vdc
Output Short Circuit−to−Ground Output Sink Current (Note 1)	I_{SC} I_{Sink}	Continuous 20	mA
Power Dissipation @ T_A = 25°C Derate above 25°C	P_D $1/R_{\theta JA}$	570 5.7	mW mW/°C
Operating Ambient Temperature Range LM293 LM393 LM2903 LM2903V, NCV2903 (Note 2)	T_A	 −25 to +85 0 to +70 −40 to +105 −40 to +125	°C
Maximum Operating Junction Temperature LM393, 2903, LM2903V LM293, NCV2903	$T_{J(max)}$	 150 150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
ESD Protection at any Pin − Human Body Model − Machine Model	V_{esd}	 2000 200	V

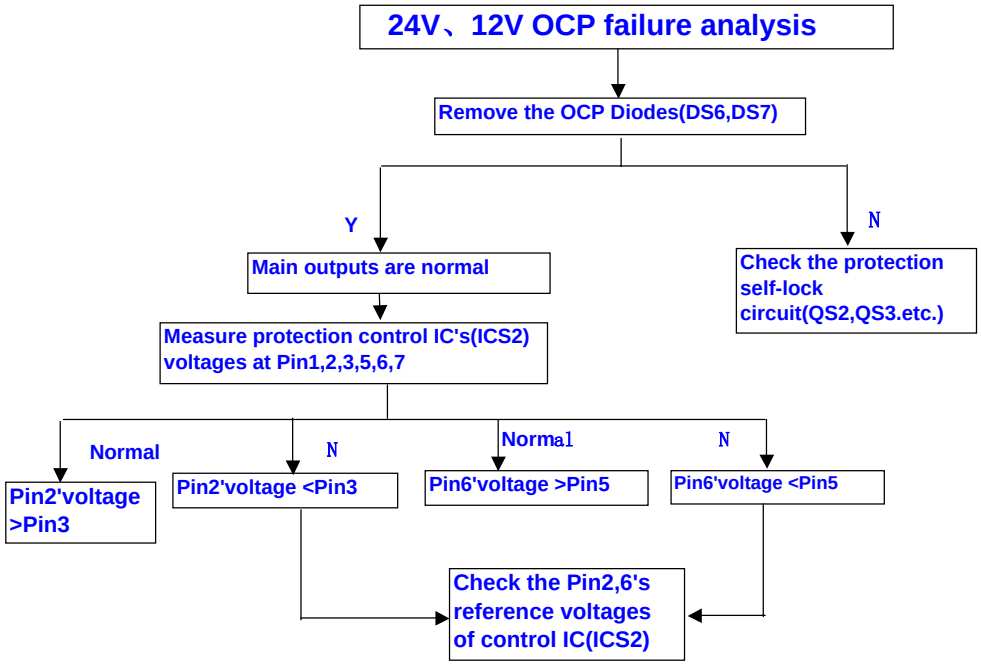
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

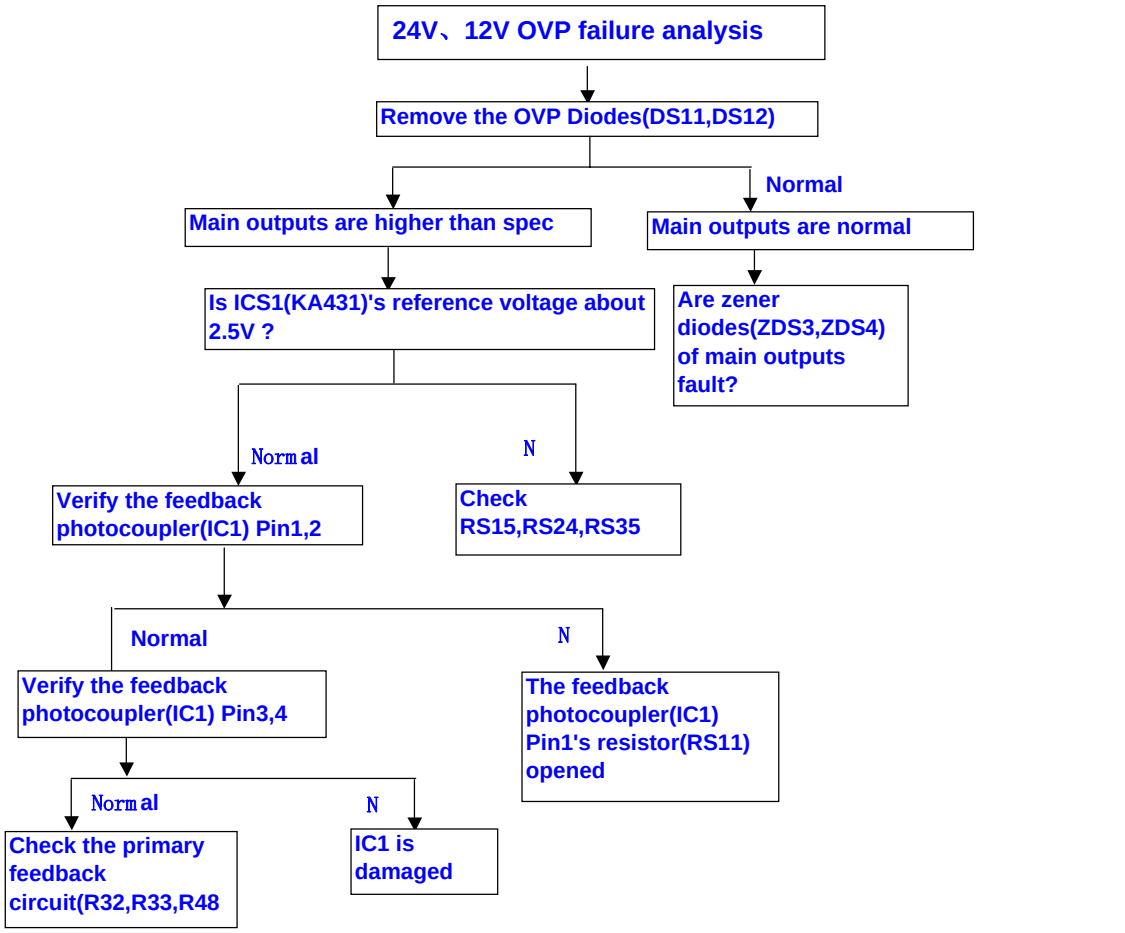
1. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}, output short circuits to V_{CC} can cause excessive heating and eventual destruction.
2. *NCV2903 is qualified for automotive use.*

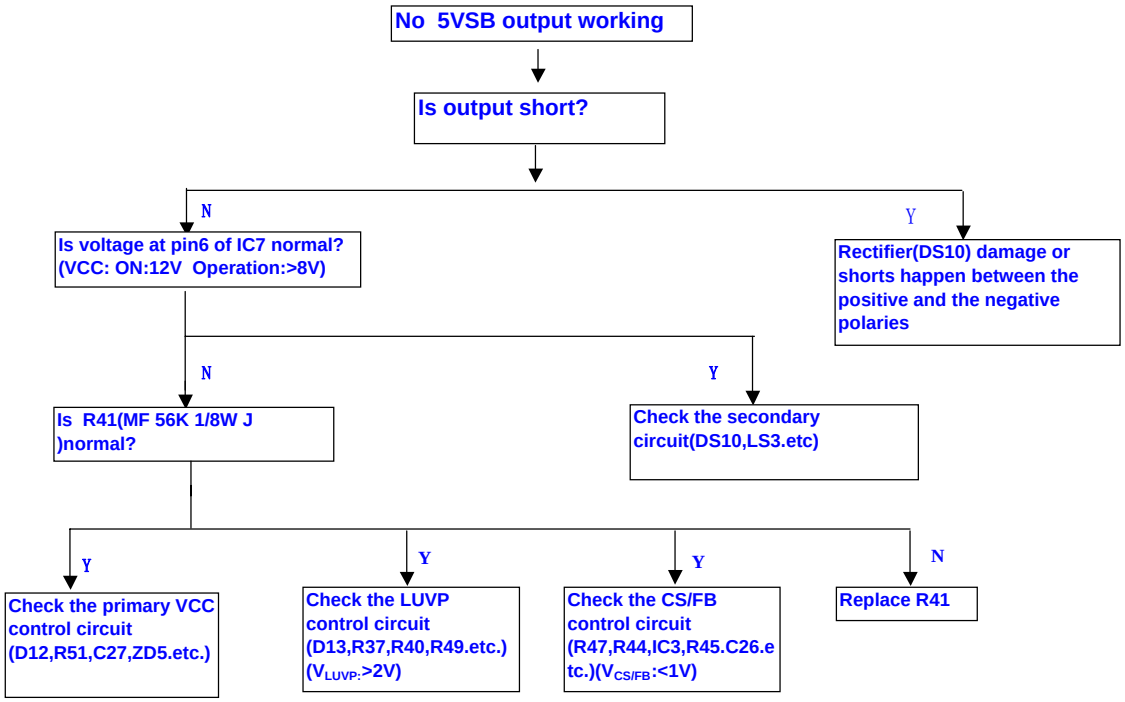
JSK4210-022B REPAIR INSTRUCTION

Repair Operation Instruction






24V、12V OVP failure analysis
Remove the OVP Diodes(DS11,DS12)
Normal
Main outputs are higher than spec
Main outputs are normal
Is ICS1(KA431)'s reference voltage about 2.5V ?
Are zener diodes(ZDS3,ZDS4) of main outputs fault?
Normal
N
Verify the feedback photocoupler(IC1) Pin1,2
Check RS15,RS24,RS35
Normal
N
Verify the feedback photocoupler(IC1) Pin3,4
The feedback photocoupler(IC1) Pin1's resistor(RS11) opened
Normal
N
Check the primary feedback circuit(R32,R33,R48
IC1 is damaged


No 5VSB output working
Is output short?
N
Y
Is voltage at pin6 of IC7 normal? (VCC: ON:12V Operation:>8V)
Rectifier(DS10) damage or shorts happen between the positive and the negative polaries
N
Y
Is R41(MF 56K 1/8W J)normal?
Check the secondary circuit(DS10,LS3.etc)
Y
Y
Y
N
Check the primary VCC control circuit (D12,R51,C27,ZD5.etc.)
Check the LUVP control circuit (D13,R37,R40,R49.etc.) (VLUVP:>2V)
Check the CS/FB control circuit (R47,R44,IC3,R45.C26.etc.)(VCS/FB:<1V)
Replace R41