TECHNICAL TRAINING MANUAL

THOMSON CONSUMER ELECTRONICS

FOREWORD

This publication is intended to aid the technician in servicing the CTC203 television chassis. It will explain the theory of operation, highlighting new and different circuits associated with the digitally controlled chassis. The manual covers power supplies, horizontal and vertical deflection, tuner, video signal processing, and audio signal processing theory of operation along with practical troubleshooting tips and suggestions. It is designed to assist the technician to become more familiar with chassis operation, increase confidence and improve overall efficiency in servicing the product.

Note: This publication is intended to be used only as a training aid. It is not meant to replace service data. TCE Electronic Service Information for these instruments contains specific information about parts, safety and alignment procedures and must be consulted before performing any service. The information in this manual is as accurate as possible at the time of publication. Circuit designs and drawings are subject to change without notice.

SAFETY INFORMATION CAUTION

Safety information is contained in the appropriate Thomson Consumer Electronics Service Data. All product safety requirements must be complied with prior to returning the instrument to the consumer. Servicers who defeat safety features or fail to perform safety checks may be liable for any resulting damages and may expose themselves and others to possible injury.

All integrated circuits, all surface mounted devices, and many other semiconductors are electrostatically sensitive and therefore require special handling techniques.

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Contents

INTRODUCTION

The **"CTC203"** series chassis is Thomson Consumer Electronics latest core-line chassis. Consumer operation and majority of features of the CTC203 series chassis are very similar to previous ProScan, RCA and GE chassis. Menu structures will be recognizable to any previous TCE product user.

Although there are differences, the component designations on the CTC203 series chassis are similar to designations on previous chassis. Most components are labeled on the circuit board. To save space the first numbers from the schematic may be dropped off. Q14100 may become Q100 or Q4100. However, it will probably be located in the 14000 series component area. In TCE Service Literature, 2 number components (R16) are generally located on the top of the circuit board, while 3 number components (C523) are located on the bottom of the chassis.

It is important for the technician to understand the difference between switching transistors and amplifiers. When switching transistors are "On", they have a very low emitter-collector voltage drop, typically 0.1–2.1 volts. Transistor amplifiers are normally biased "On" at all times and while the base-emitter voltage drop will be similar, (very close to 0.6 volts), the emitter-collector voltage drop can be from around 1 volt up to the power supply voltage.

Although this Training Manual makes every effort to follow the service data template for component location and identification, always consult the Basic Service Data (ESI) for up-to-date information. The component type (transistor, resistor, capacitor...etc.) is designated by the way the component is labeled in both Training and Service Data material.

CTC203 training material will include nomenclature that differs somewhat from previous manuals. To designate individual pin assignments of an IC, the following will be shown;

U13101-5 designates IC U13101, pin 5.

Q14608-B indicates the base lead of transistor device Q14608.

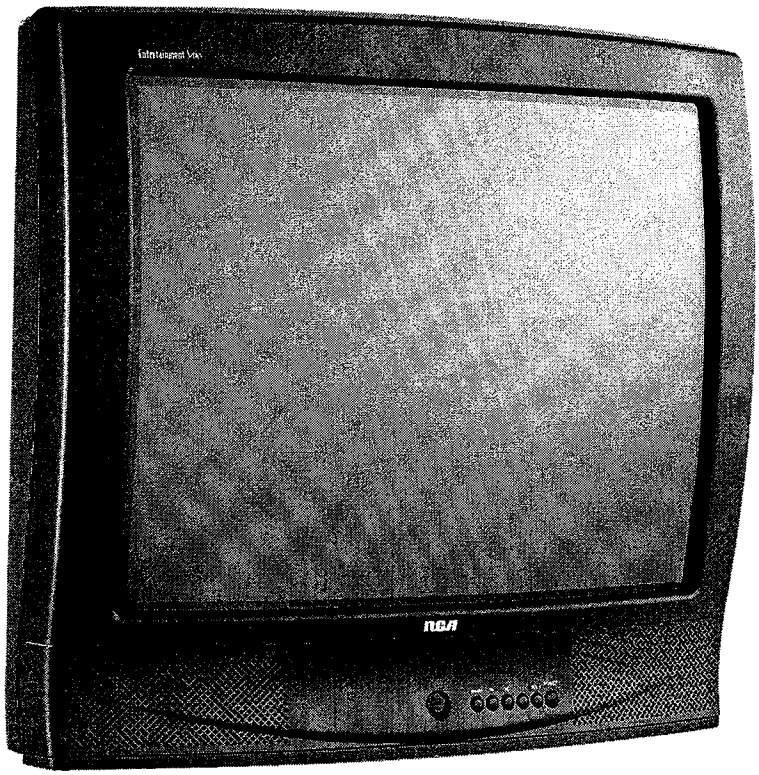
Q14601-G indicates the gate of MOSFET device Q14601.

Power supply voltages and labels will be used whenever possible. +5Vr identifies the positive 5 volt run supply. There are various classes of power supply indicators for the CTC203. They should be self-explanatory to experienced technicians, but may differ slightly from designation used in TCE Electronic Service Data. The common designations are:

- s - Standby
- r - Run
- Reg B+, which can be standby or run
- t - Tuner

Pay attention to which power supply is being referred to and confusion will be avoided. A standby supply may also provide run current.

The CTC203 uses "Hot" and "Cold" grounds. Training material and service data will continue to differentiate between the two using ⏚ for hot ground and ⏚ for cold. Always use an isolation transformer when performing service on the CTC203 chassis.



Chassis Description

The CTC203 chassis will be used in a variety of models and screen sizes. Important additions include a Gemstar Program Guide (Guide Plus+), V-Chip, on-board tuner, and a system control section that can be connected to Chipper Check. It also has a number of chassis configurations that give the chassis comb filter and S-Video capabilities. Active pincushion can also be switched in and out to accommodate large picture tubes.

While the CTC203 is versatile, most major circuits are not new, but refinements of existing designs modified to work together in the CTC203 chassis. For example, the switch mode power supply is very similar to that of Thomson's MM101 chassis, the tuner section is close to the CTC175/6/7 chassis family, and system control will look and operate much like the CTC197 chassis. Keep in mind there will be differences in symbol numbers and values of some components will change, but the basic design is the same.

The CTC203 is expected to be a "workhorse" chassis, possibly replacing all CTC176/177/186/187 product. A commercial version (to support hospital, lodging, and educational markets) is also planned.

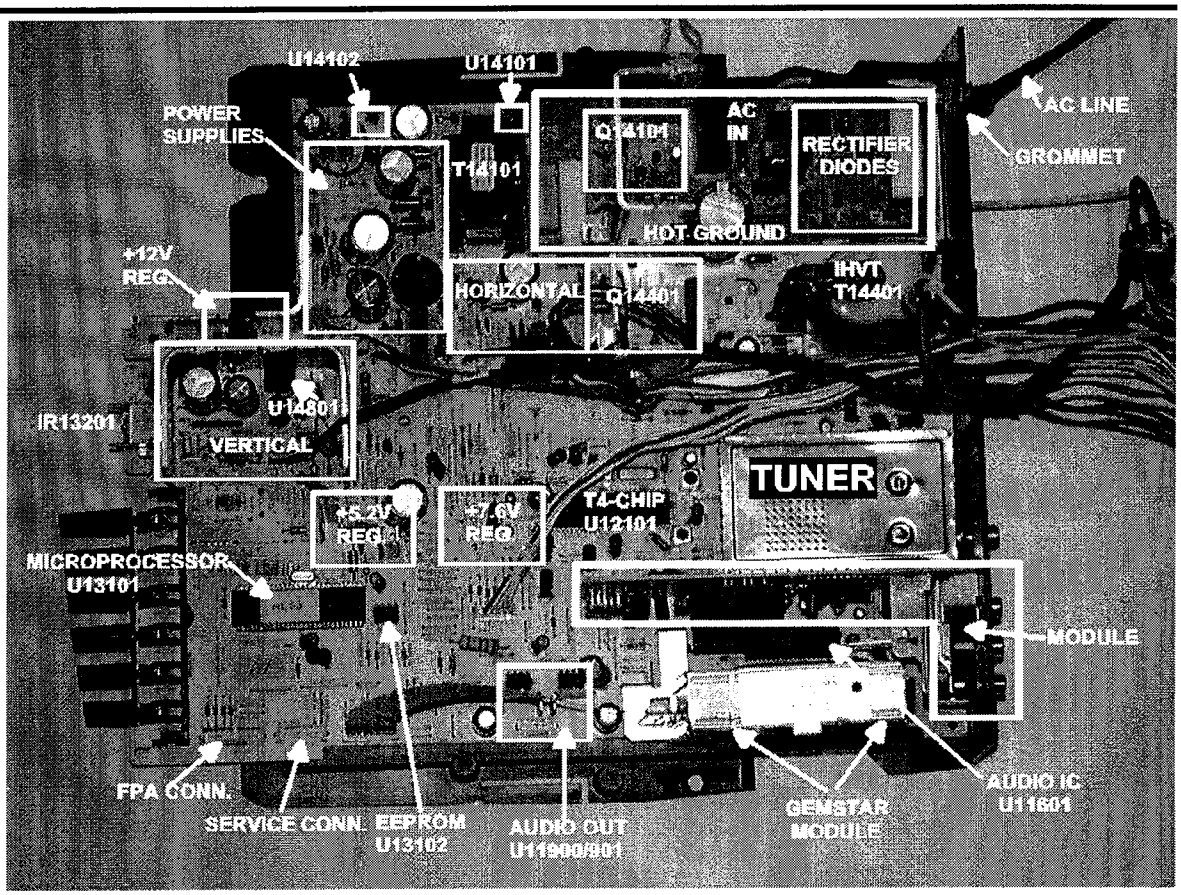


Figure 1-1, CTC203 Chassis Layout

This CTC203 Technical Training Manual will break the chassis into several major areas. Those areas are:

- Main Power Supply
- Scan Generated Power Supply
- Horizontal Deflection
- Vertical Deflection
- System Control
- Tuner
- IF
- F2PIP
- Video Module
- Video Processing
- Analog Comb Filter
- CRT Management
- Audio
- GEMSTAR
- Chipper Check

Following the main discussions are several appendices which include pinouts of the major IC's, overall block diagrams of System Control, Video Switching and Audio Switching, a glossary of new and old terms used with the CTC203 and TCE chassis in general and circuit board/component interconnect diagrams.

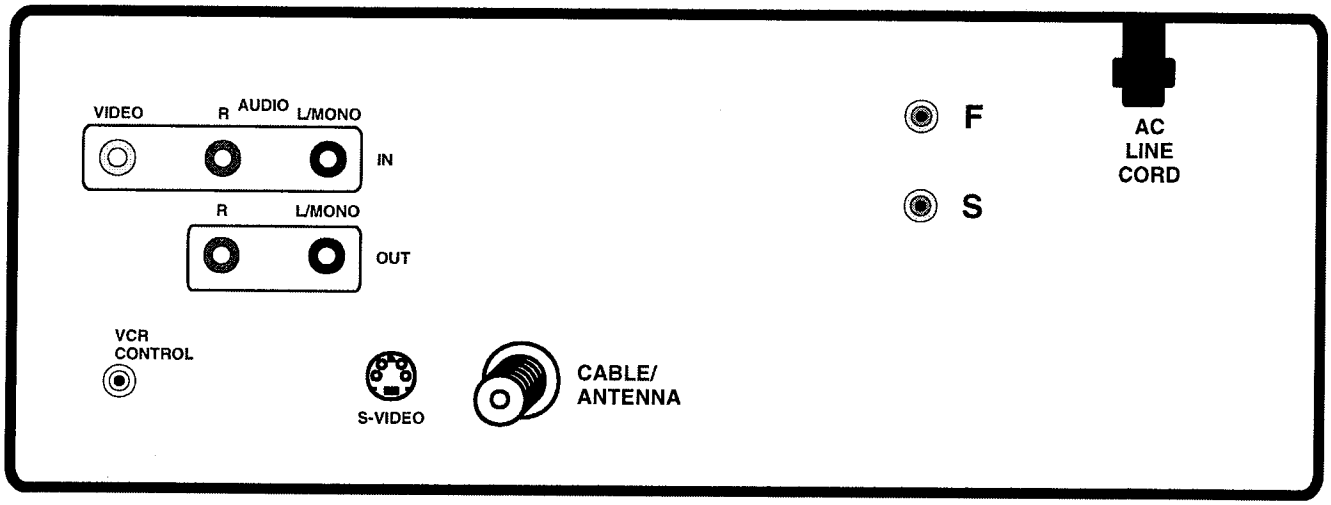


Figure 1-2, CTC203 Rear Panel

Rear Jack Panel

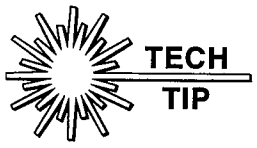
The CTC203 rear jack panel consists of three versions. One, shown above has audio/video input and audio output jacks (5J). One has only audio/video inputs (3J) and another has no audio/video input or output jacks (0J). All models have an RF cable/antenna connecter and the VCR Control connection.

The VCR Control connector enables the Guide Plus software to control a VCR or Cable Box to either automatically tune to the selected Guide Plus channel or begin recording a show selected in the Guide Plus menu.

Five jack (5J) models also have an S-Video input. If an active S-Video signal is detected, the video input will automatically switch to the S-Video source.

The screen and focus adjustments are accessible from the rear panel without removing the back of the set.

The Guide Plus+ software has a special learning/demo mode available to the consumer. Most sets contain a pin inserted into the VCR CONTROL jack on the rear panel of the set automatically enabling this mode. The pin activates the mode every time the set is turned on. Although the set immediately enters the demo mode it can be taken out via on-screen menu selection. However, as long as the pin is the rear panel jack, the set will not receive channels above VHF 13 whether the demo mode is active or inactive. The set must be turned off, the pin removed and the set turned back on for normal operation to return.



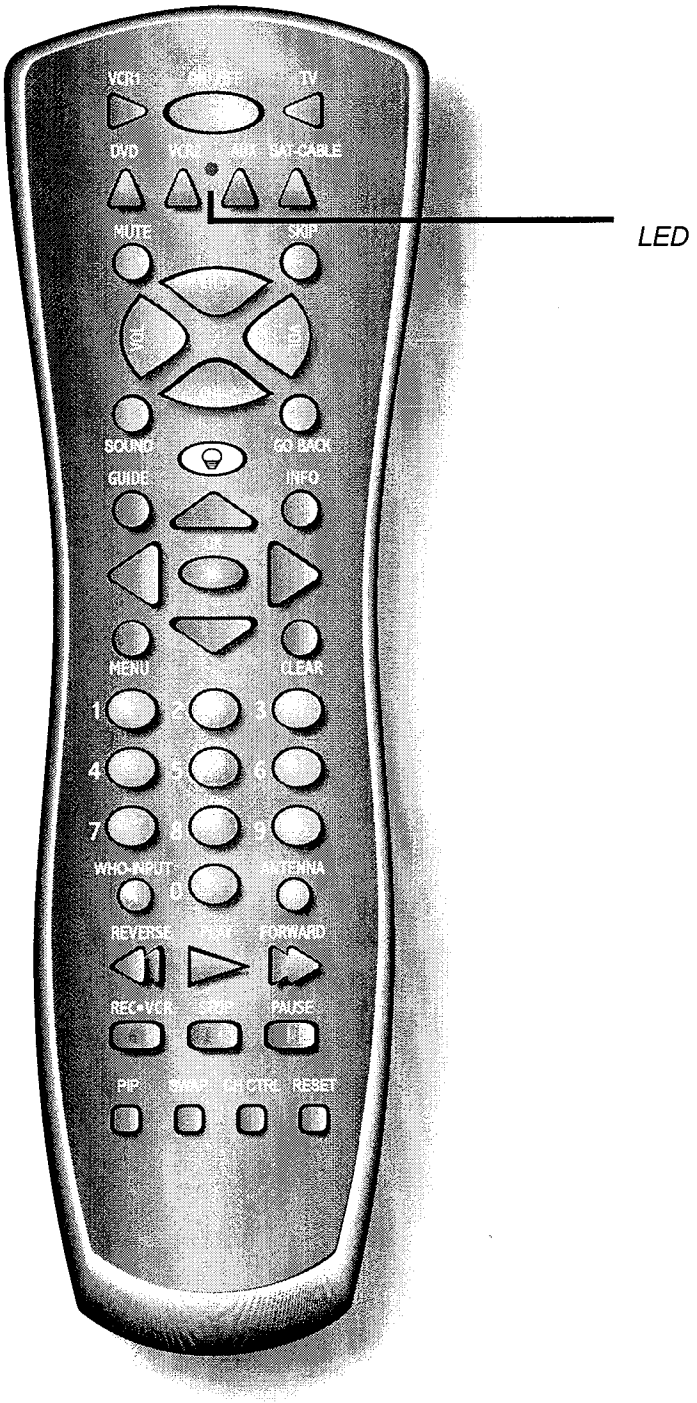


Figure 1-3, CRK76E1 Remote Control

CRK76 Remote Control

Although similar to previous remote controls, the CRK76 remote for the CTC203 has a few added capabilities. Carried over are the "navigation" buttons located in the middle of the remote. Instead of using "Channel Up", "Channel Down", "Volume Up" and "Volume Down" to navigate through the on screen menu structure, these navigation buttons will be used. The user will point using these buttons, then press "OK" to select the desired instruction. They are also essential to the use of the Guide Plus+ menu system.

The CRK76 series used in the CTC203 is also a "universal" remote capable of controlling current equipment such as VCR's, Cable Boxes, and Satellite Receivers from most major consumer electronics manufacturers. In addition, the remote may be programmed to control RCA and RCA Dimensia audio equipment and RCA, GE and PROSCAN DVD players.

Remote Control Operation

Normal remote functions will not be discussed. These functions have not changed over the last several remote control models. The following text explains new buttons and their functions.

LED: Indicates the remote is in "Learning" mode when programming the remote to be used with other equipment.

SOUND: With one press brings the user directly to the audio processor menu.

Guide: Accesses the Guide Plus+ menu. When the remote is programmed to control the SAT-CABLE equipment, accesses any available on-screen menus for those devices.

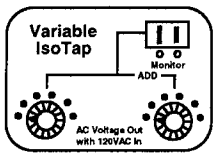
GO BACK: Returns the user to the previous channel selection, or if in MENU, returns to the previous menu selection.

WHO-INPUT: Toggles through all available input sources.

SAT-CABLE: Places the remote in control of a compatible satellite receiver or cable box. If Auto-tuning is enabled, also will turn on the TV and select the correct input to display.

Some buttons and functions are not available on every model equipped with a CTC203 chassis. For instance, on models without PIP, the bottom four buttons on the remote will not be present. Some models of the remote do not include back lighting and on some models only the volume and channel buttons illuminate. Always consult the latest ESI™ for the correct remote part number for a particular chassis prior to ordering a replacement.

SERVICING PRECAUTION!



Most ground connections on the CTC203 series chassis are cold, (⏚), indicating they are isolated from the AC line. However, there are many **"Hot"** connections, (⏚), meaning direct connection to the AC line. The AC input and primary side of the power supply circuitry are examples.

Always use an isolation transformer

and consult service data when performing service on this chassis and other chassis in this family!

Power Supply Overview

There are three power supplies providing power to the CTC203. All derive power from Raw B+ and/or Regulated B+. They are:

- Standby
- Run (Switched)
- Scan Derived (High Voltages)

Due to higher power requirements of the CTC203, the power supply takes a new approach to meet the higher loads. Primarily, the main supply operates in "forward" conduction mode, delivering power to the secondary transformer windings during power transistor "on" time when the magnetic fields are expanding, rather than during "off" time when the fields are collapsing.

All standby supplies also ramp up to supply the current demands of the chassis during run operation. Derivations of the main supply also provide current for the scan derived and the switched supplies.

There are three modes of operation for the main supply but only two for the switched and scan derived supplies. They are:

- Standby
- Data Acquisition
- Run

The main power circuits supply many different voltages to the CTC203 chassis. Figure 2-1 is a block diagram showing the voltages generated and their derivations from the main power. Notice all standby voltages are derived from Raw B+. However, differing from most previous chassis', the main supply generates all low voltages required during Run, Standby and Data Acquisition modes of operation. All voltages, except the switched and scan derived, are available any time the AC is connected to the line. Mainly, they supply the microprocessor, infrared remote control detection and tuning circuitry during standby. All other voltages are derived from the main supply and switched on during run or data acquisition modes.

The main supply generates voltages for normal operation of all other circuits and components. In addition, many of the supplies are used to generate the remainder of the low and high voltages required by the chassis.

The Technical Training Manual will discuss the power supplies in this order; Main, Switched (SW) and Scan Derived.

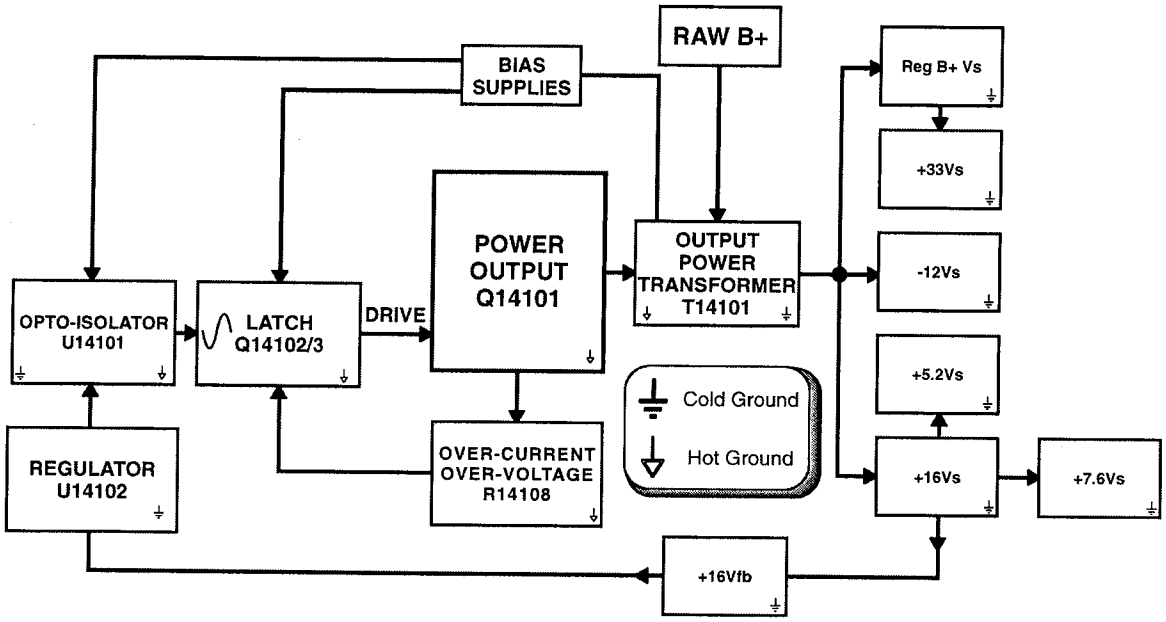


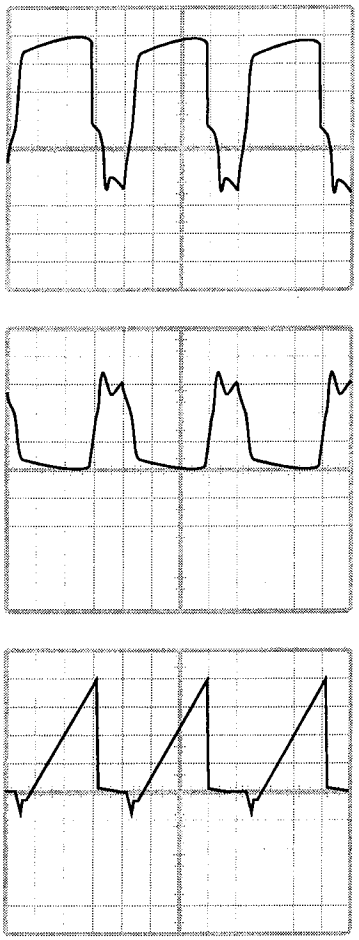
Figure 2-1, CTC203 Main Power Supply Block Diagram

Standby Supply Overview

The standby supply is a new class of high power, ZVS (*Z*ero *V*oltage *S*witching) supply developed to minimize switching losses and radiated noise. A return to discrete devices lowered parts count and decreased circuit board space utilization.

ZVS refers to the ability of the supply causing the voltage across the principal power output device, to reduce to near zero before the device is switched on. Yet it has a slow enough time lag to allow the device to switch off completely before any appreciable voltage is present across the device. This can better be illustrated in Figure 2-2.

Note that the first two waveforms are voltages, while the third is current. The MOSFET begins conducting current when the gate voltage reaches the proper turn on point. From that time, output current rises linearly due to the inductance of the output transformer. However, notice that once the gate voltage goes high, the drain voltage decreases almost to zero volts. This eliminates much of the heat dissipation normally required of an output device.



By reducing the switching losses to almost zero, the efficiency of the power supply is greatly increased and the limiting of the switching voltages causes a substantial reduction of switching noise.

Also note that by utilizing the resonant recapture of energy stored in the leakage inductance of the output transformer, neither a snubber nor a clamp is required, leading to improved efficiency and lower parts count.

Figure 2-2, Power Supply Output Device Waveforms

Digital Latches

Before wading deeper into the CTC203 power supply, the technician should become familiar with the control circuitry used to turn the power output devices on and off. It will be common to various ZVS supplies used throughout this and other TCE chassis'.

The control switches act similar to an SCR, but with a few variations. Figure 2-3 shows a truth table and simplified schematic representaion of the power supply control latch shown in Figure 2-4. Again, while the other ZVS supplies may have slight variations, the basic concept and operation is the same.

Q1 and Q2 form the basic latch circuit. Both are switching transistors that saturate when tripped on. In this case an NPN and PNP are used to force the desired results on the output. The latch is controlled by placing or removing voltages on either base while sufficient voltage is present on Q2-E to set the latch. Keep in mind B+ will supply drive to the output when the latches are off!!! The latch REMOVES the output. Any time the truth table shows a low (0) condition, output is removed.

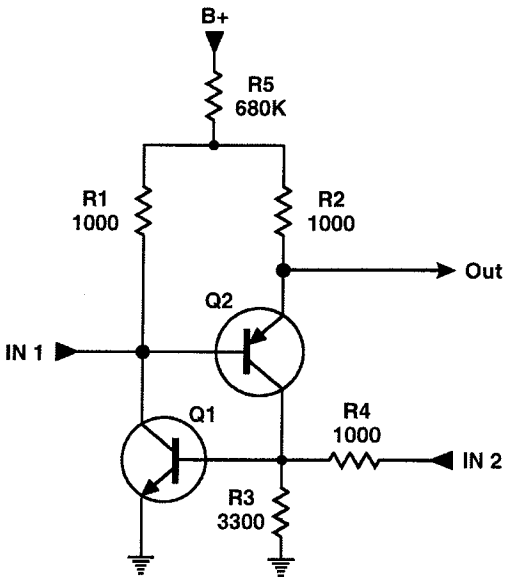
In condition A, both IN1 and IN2 are low (0). A low in Q2-B turns it on providing a current path from B+ through R5, R2, Q2-E/C and R3 to ground. Sufficient bias is developed across R3 to turn Q1 on, setting the latch. Now, regardless of what happens on IN1, the latch is set. The combined voltage drop on R3 and Q2-E/C places Q2-E at a very low voltage, shutting the output off.

If IN2 goes high (1) as in condition B, there will be no effect on the output. The high on IN2 would turn Q1 on, but since it is already on the result is no change in the output state.

In condition D, both inputs are high. A high on Q1-B turns it on. When it turns on it saturates, bringing Q2-B low, turning it on. When it turns on the latch is again set and the output goes low.

Condition C is the most difficult to understand because it relies on the input voltages being different before the latch is tripped. If IN1 is high, the latch state is dependant upon IN2 for its output state. If IN2 is low, the output is high. If IN2 is high, the output is low. However, if the latch is set (tripped) Q2 saturates and holds Q1 on even with IN1 high. What has to happen before the latch will trip off is the loss of bias on Q1-B.

As IN2 decreases it begins to divert current flow away from R3 and its voltage drop also begins to decrease. The voltage on Q1-B will eventually drop low enough for it to shut off. If IN1 is still high Q2-B is now high and it also shuts off. This removes both Q1 and Q2 from the circuit and B+ now supplies the output voltage.



	IN1	IN2	OUT
A	0	0	0
B	0	1	0
C	1	0	1
D	1	1	0

Figure 2-3, Digital Latch & Truth Table

Control Latch Review

Now that the digital latch operation is understood, it needs to be shown how it is used to regulate the CTC203 power supply. Using the simplified digital latch schematic from the previous page, when IN1 is high, IN2 may be used to control the output. When IN2 is high, the output is low. When IN2 is low, the output is high. In Figure 2-4A, Q1-E is grounded. Normal PN junction drop of a transistor dictates that a bias of at least +0.6V must be placed on Q1-B to turn it on.

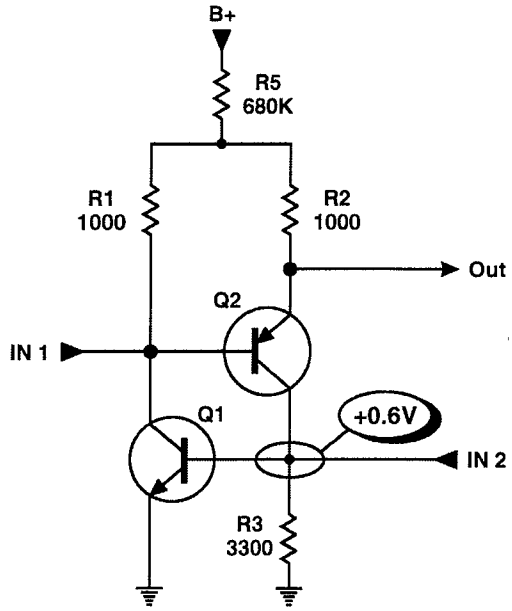


Figure 2-4A, Digital Latch Normal

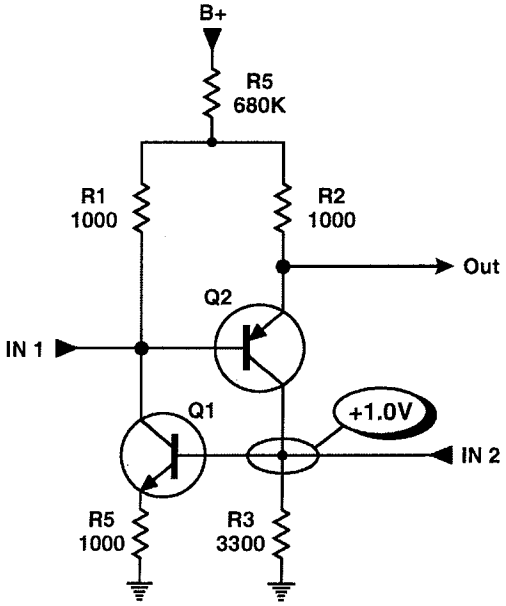


Figure 2-4B

In Figure 2-4B a resistor (R5) has been placed in the emitter circuit of Q1. The resistance of R5 reduces the amount of current through the PN junction of Q1E/B with the same voltage on Q1-B. Thus, to increase current high enough to turn on Q1, Q1-B voltage must increase. In this case to about +1.0V.

In Figure 2-4C Q1-E is connected to a negative 5V supply. The current to turn the PN junction of Q1 on remains the same. Now the voltage on Q1-B need only be 0.6V higher than Q1-E, or about -4.4V.

In this manner, the voltage that triggers Q1 may be varied and used to control the output of the latch. By understandby this circuit, the regulation and protection of the power supply may be more fully understood.

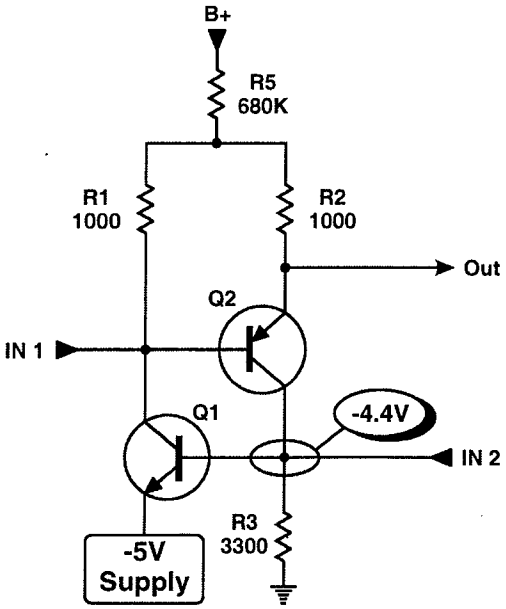


Figure 2-4C

Latch Circuit

Figure 2-5 is the control latch for the CTC203 power supply. It is not much different from the simplified schematic in Figure 2-3, however there are some additional circuits that will need to be discussed later.

When power is first applied to the chassis, Raw B+ is available on the "IN1" line at the junction of Q14103-C and Q14102-B. Since there is no bias difference from Q14102B-E, it is off and the latch is off. Raw B+ now supplies gate drive to the output device Q14101-G, turning it on providing output transformer current. At this time, "IN1" is high, IN2 is low and the latch is off, *allowing* gate drive.

As current builds in the output device, a voltage is developed accross R14108. When this voltage increases enough, it will bias Q14103 on, which also turns on Q14102, setting the latch. A current path now exists between Raw B+, R14103, R14106, Q14102-C/E, R14110 and a negative bias voltage developed from the output transformer.

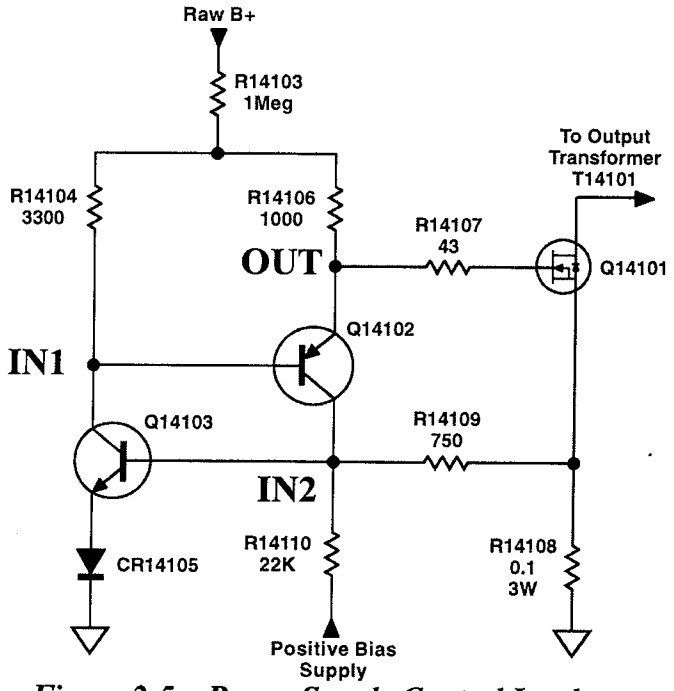


Figure 2-5, Power Supply Control Latch

Once the latch is set, Q14102-E voltage and output drive is removed and the output device, Q14101 shuts off. With output current dropping, the corresponding voltage drop across R14108 begins to decrease along with the negative bias supply. At some point the voltage at Q14103-B drops low enough to allow it to turn off. When it does, bias is removed from Q14102-B and it shuts off. When it shuts off, gate drive is again allowed to turn the output device, Q14101 on and output current begins to build once more.

As the power supply circuits develop, it will be seen that by either varying the bias voltage on Q14103-B while maintaining the voltage on Q14103-E, or varying the bias on Q14103-E, while maintaining the voltage on Q14103-B, the on/off time of the latch can be controlled precisely. Controlling the latch means output current is also controlled. The off time of the latch is reasonbly constant. It is the "on" time of the output that controls the supply voltages.

Main Supply Block Diagram

The Main Supply distributes power to all devices that need to remain "alive" when the chassis is "off". In addition, it must retain enough power to keep the microprocessor active during a power failure event long enough to exercise the "batten down the hatches" routine leading to a graceful shutdown of the chassis before power disappears completely. ("Batten" is a software routine which stores off all customer settings and chassis alignments to the EEPROM. This enables the set to start normally after a catastrophic power failure.)

The voltages available during standby operation are:

- -12 volts
- +5.2 volts
- +7.6 volts
- +16 volts
- +33 volts
- Reg B+

The supply converts raw B+ from the incoming AC line into the various DC supplies required by the CTC203. There is a "Data Acquisition" mode requiring greater current supply demands from the supply than normally needed during standby, but less than is needed during full run operation. For instance, during a TVGuide+ download, there is no reason for the set to display a picture, however, the tuner must be active to receive the signal. This requires more current from Reg B+ from which the +33V supply is derived.

Since the forward conduction mode is used, the driver current is proportional to the supply current and higher frequencies (70-90 kHz) may be used for greater efficiency.

The standby supply may be broken into several sections according to Figure 2-5. The Latch circuit (discussed previously) consists of Q14102 and Q14103. They control the off/on time of the output device, Q14101.

Current in the output power transformer, T14101, transferred to the secondary, is used to generate the various supplies from Raw B+ provided by the main rectifier from incoming AC.

The regulator, U14102 and opto-isolator, U14101 provide regulation of the +16Vs supply and isolation between the cold ground run supplies and the hot ground generator circuit components.

Overcurrent and overvoltage protection of the output device is provided by resistor R14108 in series with Q14101.

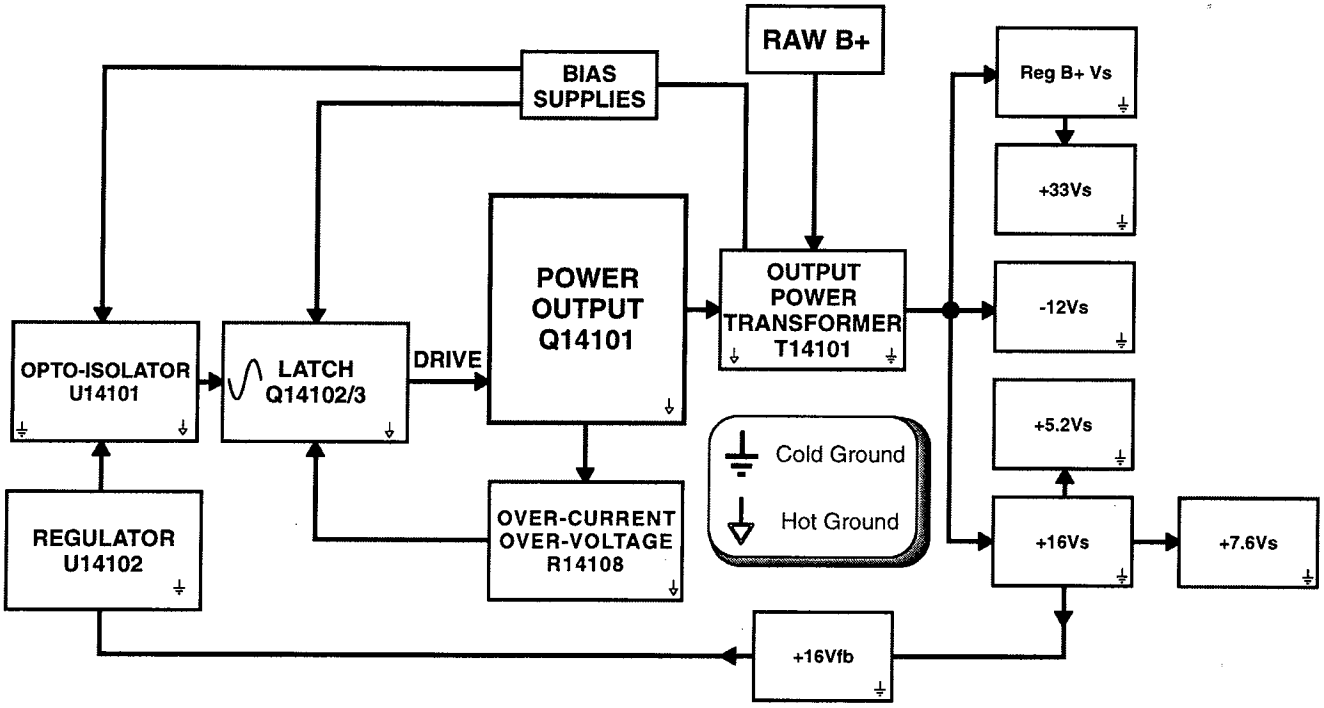


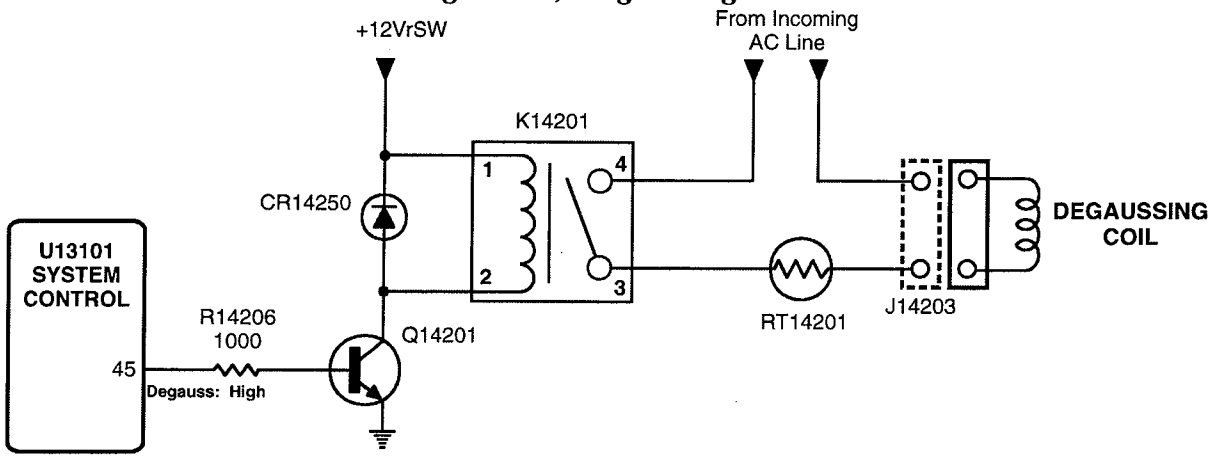
Figure 2-6, CTC203 Main Supply Block Diagram (Stanby Voltages)

AC Input and Degaussing

Raw AC is connected using protection (F14200) and filtering/smoothing components to assure spikes and unexpected surges do not cause catastrophic failure.

Degaussing may only be done when the +12V run supply is active. System Control sends a high out during startup turning on Q14201. As long as the +12Vr supply is up, relay K14201 is turned on activating the contacts on pins 3 & 4. Current from the AC line is now routed to the degaussing coil. Degaussing occurs as long as thermal resistor RT14250 allows. It provides an exponential decay of current to the degaussing coil. Degauss current must be allowed to decay before the relay stops all degauss coil current to allow proper degaussing, otherwise color non-uniformity will result. When System Control removes the active deguass signal, Q14201 shuts off, removing drive current from the relay coil, breaking the contacts and removing AC power from the degaussing coil. The degaussing cycle is then complete.

Figure 2-7, Degaussing



Raw B+

Incoming AC (95 - 135 VAC) is input through an LCI (Line Conducted Interference) filter consisting mainly of T14201 and several filter capacitors. Raw B+ is generated from the incoming AC by a discrete bridge rectifier circuit consisting of CR14201, CR14202, CR14203 and CR14204. Main power supply input voltage is 95-135 VAC to provide a Raw B+ voltage of about +156V depending upon the chassis version. Generally, larger screen sizes will require higher raw B+.

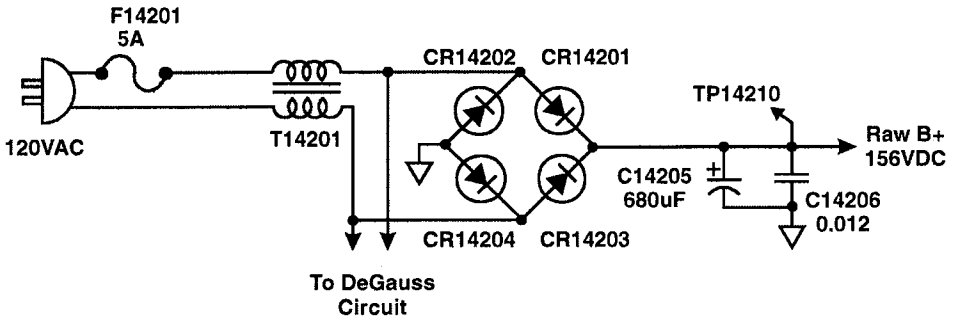


Figure 2-8, AC Input

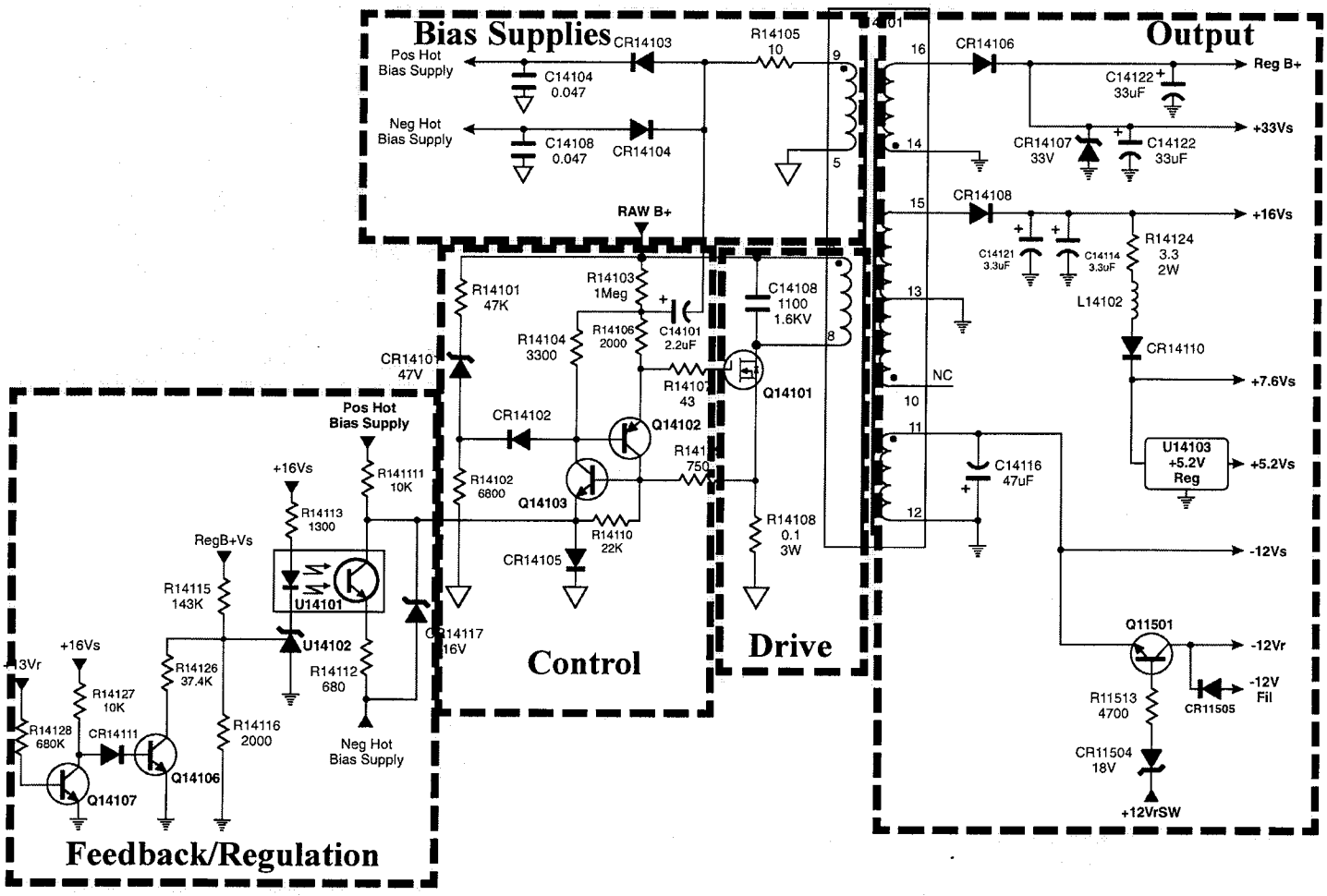


Figure 2-9, Main Power Supply

Main Supply Operation

To simplify the understanding of the standby supply (shown in Figure 2-9), it will be broken down into smaller blocks. These blocks operate somewhat independently, but ultimately must all function together for proper operation of the supply.

The sections are:

- Output
- Drive
- Control
- Feedback/Regulation
- Bias Supplies

Standby Supply Startup

A voltage divider network from Raw B+ consisting of R14103 and R14107 provides the initial positive gate voltage for output MOSFET Q14101 to begin conduction. As current begins to flow in the output transformer T14101, winding 3/8, feedback current is induced to windings 1/2. This winding provides several bias voltages to the supply drivers and feedback circuit, but initially is used to increase the gate voltage, using C14101 to couple the transformer to the gate. The voltage at pin 9 is increasing in a positive direction as current increases in the primary. This rising voltage eventually causes the output, Q14101, to saturate, beginning the first cycle of operation.

As current through Q14101 increases, the voltage drop across current sense resistor R14108 increases until a threshold is reached. (This threshold is discussed in the control latch section.) At the time the threshold is reached, the regenerative switch (latch circuit) consisting of Q14102/Q14103 turns on, removing gate drive from output device Q14101.

Current flow through Q14101 drops quickly to zero and energy stored in the transformer primary winding is transferred to C14108 which charges with the negative potential at Q14101-D. This rising voltage appears across the secondary winding.

When the secondary side of the transformer conducts, the energy stored in the primary of T14101 is delivered to the secondary supply capacitors and the load. After the secondary diodes stop conducting, energy still contained in C14108 drives the drain voltage of Q14101 toward zero. When the drain voltage attempts to go below zero, an internal diode clamps it near ground.

Now the voltage of T14101 drive winding, 5/9, goes positive and if the latch circuit allows it, will turn on Q14101 and the next cycle begins. Once the initial startup pulse from Raw B+ starts the cycle, this bias supply takes over and continues to supply gate drive to the output device.

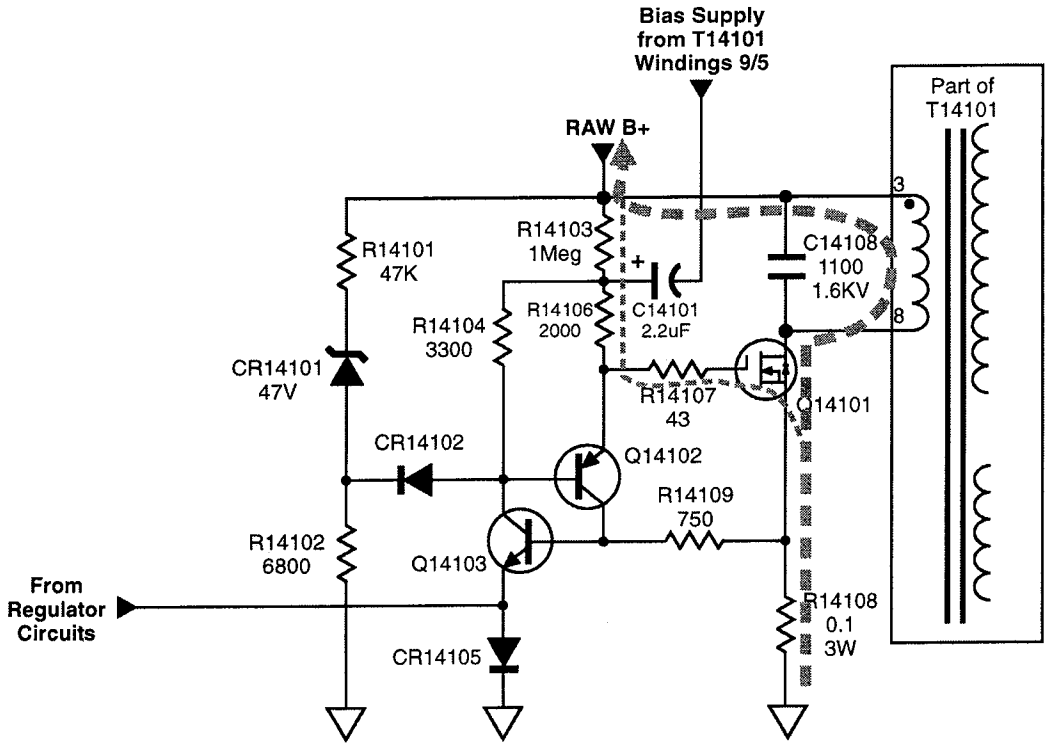


Figure 2-10, Power Device Start up Current Flow

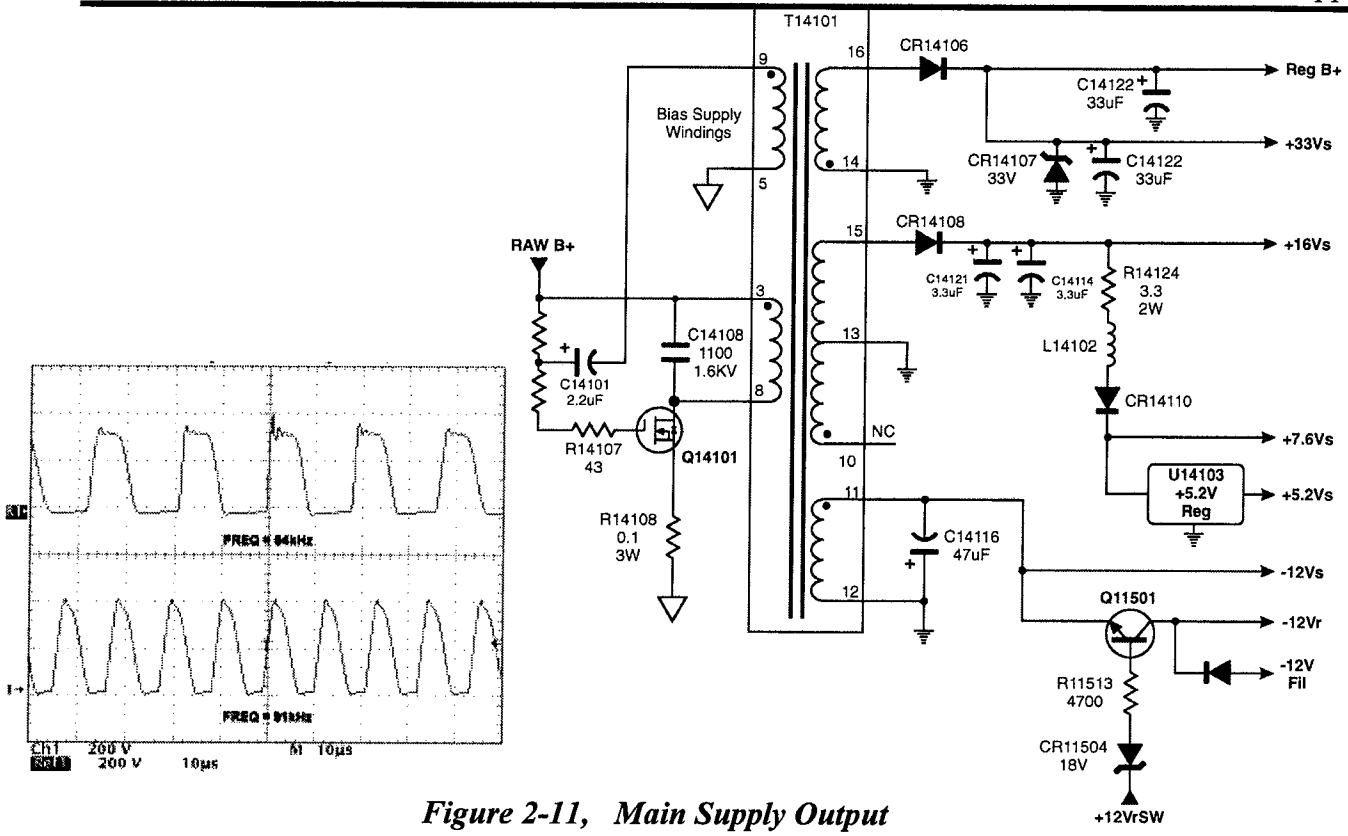


Figure 2-11, Main Supply Output

Output

Q14101 provides all transformer primary winding drive current. It is a power mosfet which conducts current from source to drain when the gate voltage is high. Once on, gate voltage must be reduced to around zero or the drain-source current path must be interrupted to stop output current. During conduction, current flows from common (hot) through R14108, Q14101 and T14101 primary winding to Raw B+. C14108 is used to "tune" the resonant frequency of the primary for better power transfer. Normally this frequency is around 90kHz during standby and 40-60kHz during run operation. Figure 2-11 shows the driver and output voltages and a waveform comparing Q14101-D outputs in standby and run mode. As current flows through the primary, flux lines induce current flow into secondary windings 5/9, 11/12, 13/15 and 14/16. Typical AC voltages generated from the windings are shown in Figure 2-12.

T14101 Pin #	AC Voltage
3/8	400 p-p
5/9	15 p-p
11/12	26 p-p
13/15	35 p-p
14/16	250 p-p

Figure 2-12, Typical Secondary Winding Voltages

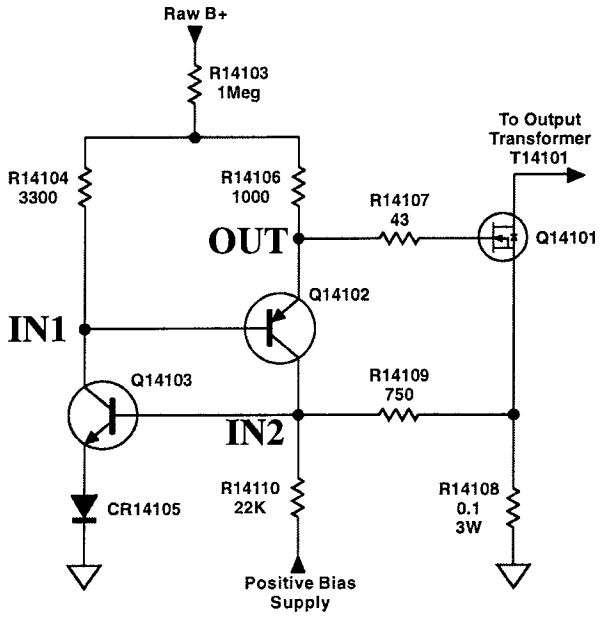


Figure 2-13, Main Supply Output Drive Control

Standby Supply Drive

To assist the understanding of the control circuit, this discussion will not take the positive bias supply in consideration at this time. Operation of the control circuit will be identical.

At initial startup, R14103 provides the gate voltage to turn Q14101 on, providing primary current. As Q14101 begins to conduct, primary winding current increases, increasing voltage across the winding and inducing current flow to all secondary windings. Q14101 quickly saturates.

R14108 monitors the primary winding current, which is also the current through the output device, Q14101. As this current increases, the corresponding voltage drop across R14108 increases. When it reaches a voltage high enough to turn Q14103 on, the latch "sets" stopping drive to the output, Q14101. It does this do to a current path from common through CR14105, Q14103-E/B, Q14102, R14106 the gate drive being developed by C14101 and T14101 windings 5/9. Q14102 emitter drops to a low voltage, shutting the output device Q14101 off. This cuts current flow to the primary of T14101. Without drain current, drain voltage now increases due to back EMF across the transformer windings. The secondary diodes conduct and power is delivered to the loads. C14108 helps shape the waveform, limiting conduction time as Q14101 shuts off and drain voltage is driven to zero.

Two things are now happening. First, with Q14101 now off, primary current flow begins to decrease. Second, with current flow in the primary and output stopped, the voltage across R14108 now decreases below the bias point of Q14103 and it shuts off, shutting off Q14102. The bias supply developed from T14101-5/9 and C14101 now supplies gate drive and the output, Q14101 turns back on. The process now begins again.

Bias Supplies

There are two supplies generated during standby supply operation used to internally bias the control and regulation components of the supply. Both cycles of the transformer waveform are utilized to provide a positive and negative supply voltage. These voltages vary with respect to the current flow in the primary winding of T14101 but should normally be within the 5 to 10 volt range, positive and negative respectively. An unrectified pulse is used as the initial gate pulse to saturate the output device.

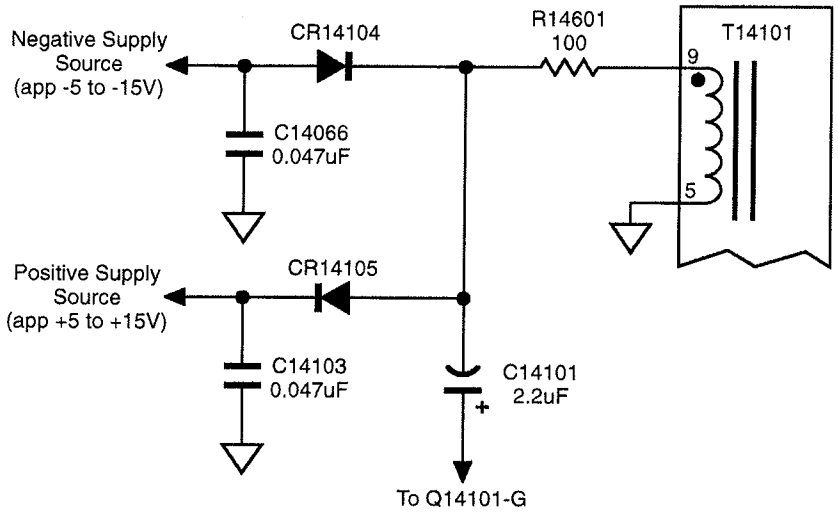


Figure 2-14, Bias Supplies

Standby Supply Control

Without some form of regulation, the power supply will quickly reach a nominal output voltage using the control circuit in Figure 2-13. Figure 2-15 again shows the control circuitry, but adding regulation to keep the output voltages from the secondary of the supply within design limits. Load variations are constant and there is the problem of loads outside the normal expected variations to deal with. The main supply is required to provide standby and run power to some circuits, further complicating load demands.

All this means that the supply must be regulated and protected against overload conditions. An opto-isolator protects the "hot" primary side of the supply from the "cold" secondary side and is also used for regulation.

Referring back to Figure 2-13, it may be seen that by varying the on/off time of the latch, Q14102 and Q14103, output current can also be varied. For instance, the trip voltage required to turn Q14103 on with diode CR14105 in its emitter circuit is about +1.2V. This assumes a PN junction IR drop of 0.6V for the diode and 0.6V for the emitter-base junction of the transistor. If a second diode were placed in series with CR14105, the trip voltage would now be +1.8V. (Of course, with the added IR drop of R14109, the voltage would need to be greater.) If CR14105 were removed, the trip voltage now would be lower by 0.6V or about +0.6V.

Now it can be seen that regulating the output current by varying IN2 is a matter of either increasing the voltage on Q14103-B, or lowering the voltage on Q14103-E. Either method achieves the same results. This technique may be used to provide regulation of output current.

Main Power Supply Regulation

To provide regulation of the control latch which in turn varies the secondary voltages, a regulation circuit is used. Since the regulator is monitoring secondary voltages which use "cold" ground, and manipulating circuits on the primary or "hot" side of the power supply transformer, the regulator must also provide isolation.

Initially, a bias voltage is set up on Q14103-B by a voltage divider network between the positive and negative bias supplies. R14112, the output of U14101 and R14111 make up this network. Since the supplies are constantly changing do to primary current, they are difficult to measure, however when operating normally the nominal voltage on Q14103-B is very close to zero.

A feedback voltage, Reg B+, is used to monitor the secondary voltages generated by the main supply. If Reg B+ increases such that the junction of R14115 & R14116 rises above +2.5 volts, the internal impedance of U14102 (See the Tech Tip on this new device) decreases. Increased current through the device turns on opto-isolator, U14101 harder and the output impedance of this device decreases. This output is in the voltage divider network between the negative and positive bias supplies. As the impedance decreases, the voltage on Q14103-E goes more negative. It now takes less voltage on Q14603-B to trip the control latch to the "ON" condition. Remember that when the latch is on, gate drive is removed from the output device, Q14101, and output current stops. Secondary supply voltages begin to drop.

The waveform shows voltage levels on the emitter of U14101 (Top) and the collector (Bottom). The emitter is essentially the negative supply ripple. The DC level is about -11V. The internal impedance of the output section is increasing and decreasing at such a rate that under normal load levels it fluctates closely around 0V.

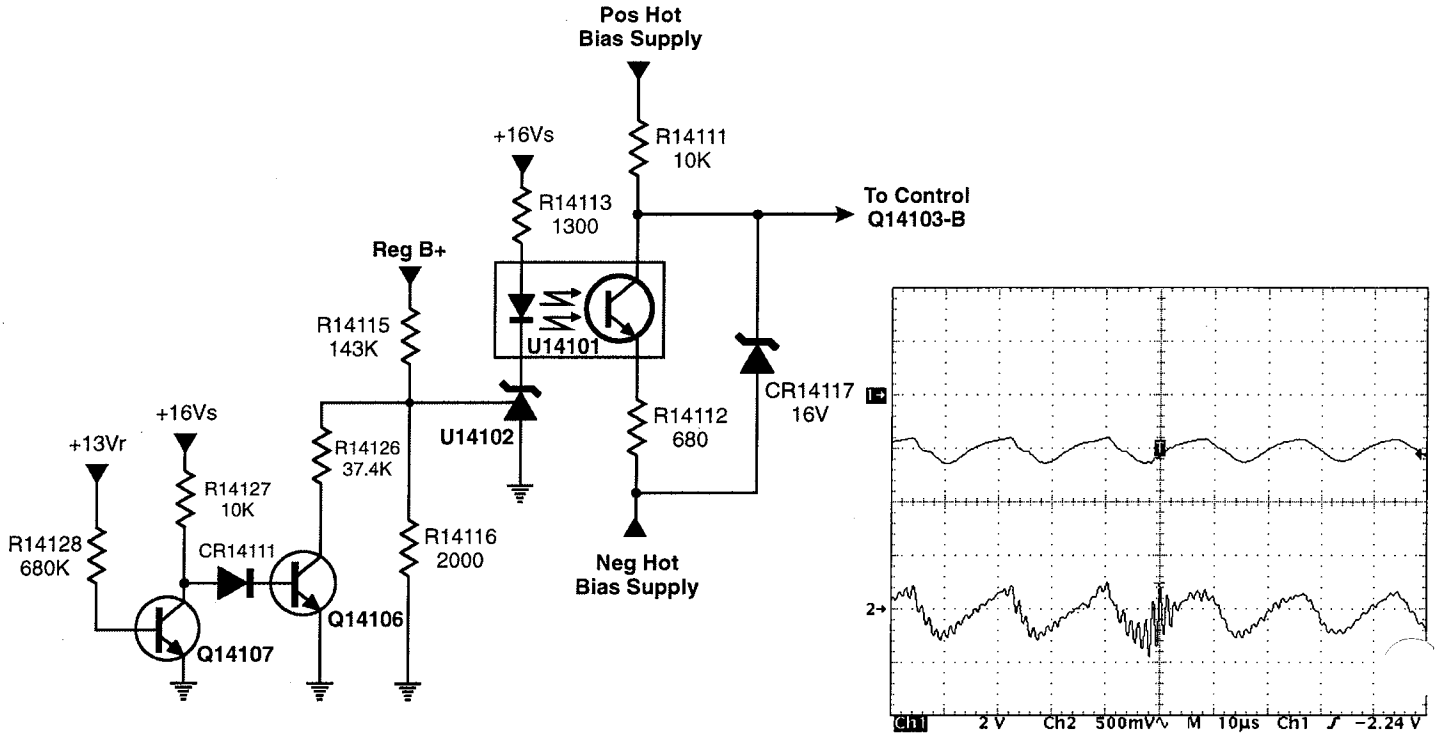


Figure 2-15, Standby Supply Regulation

When Reg B+ drops sufficiently, the junction of R14115 & R14116 drops below +2.5V. Now the internal impedance of U14102 increases. As it increases, the output section of the opto-isolator, U14101 is driven less and its impedance also increases. The voltage on the collector of U14101 now goes towards the positive supply. This voltage is also on Q14103-E. It now takes more voltage on Q14103-B to turn the control latch off. Gate drive is allowed on the output, Q14101 and primary winding current is again available in T14101. As current in the primary increases, voltage in the secondaries also increases and the cycle repeats.

If a failure occurs in the regulation circuits such that the output of U14101 opens, the positive hot supply is placed on Q14103-E. Output current is now stopped only by the overvoltage/overcurrent protection provided by R14108, which is acting as a current monitor for the output device.

If the failure mode shorts U14101 output or places it in a low impedance mode, the negative hot supply, only limited by R14112 appears on U14101-C and thus Q14103-E. It now takes very little output current to trip the latch and remove output drive. All supplies will be reduced and not maintain any regulation.

Precision Shunt Regulator

TECH TIP

The three terminal precision shunt regulators used throughout the various supplies of the CTC203 are unique devices. They may be thought of as "gated" zener diodes, or infinite gain operational amplifiers with a reference voltage tied to the negative input. In both cases, for the CTC203 chassis, 2.5V is the reference voltage.

Figure A shows the regulator when the reference voltage on pin 1 is above 2.5V. The regulator conducts, its internal impedance decreases, and current through the device increases.

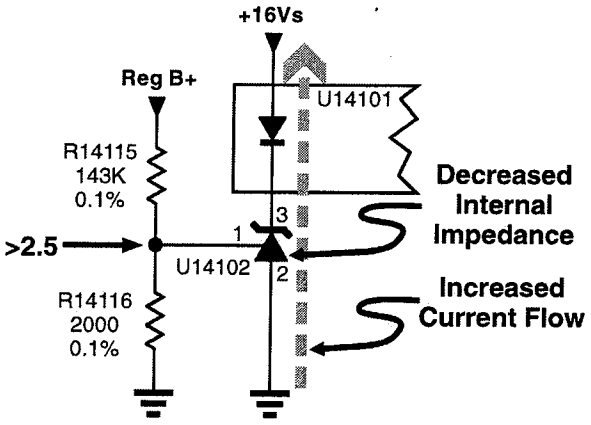


Figure A

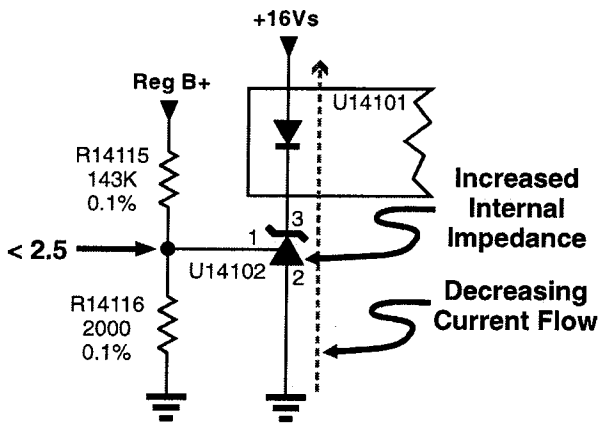


Figure B

Figure B shows the regulator when the reference voltage on pin 1 is less than 2.5V. The internal impedance of the regulator increases and current flow through the device decreases.

In both cases, the current through the regulator directly drives the LED side of the opto-isolator. As this current increases, the output impedance of the opto decreases. As current decreases, the output impedance increases.

Run Mode

In order to supply the different current demands between standby and run modes, the main supply monitors the +13Vr supply generated from scan. If the supply is running, Q14107 is on, turning off Q14106. This removes R14126 from the regulator circuit and supply operates normally.

When scan is lost, the +13Vr supply is removed turning off Q14107. This turns on Q14106 placing R14126 in parallel with the second regulator network resistor R14116. This effectively lowers the resistance of the pair. It takes less Reg B+ voltage to trip the latch and current in the output transformer is decreased.

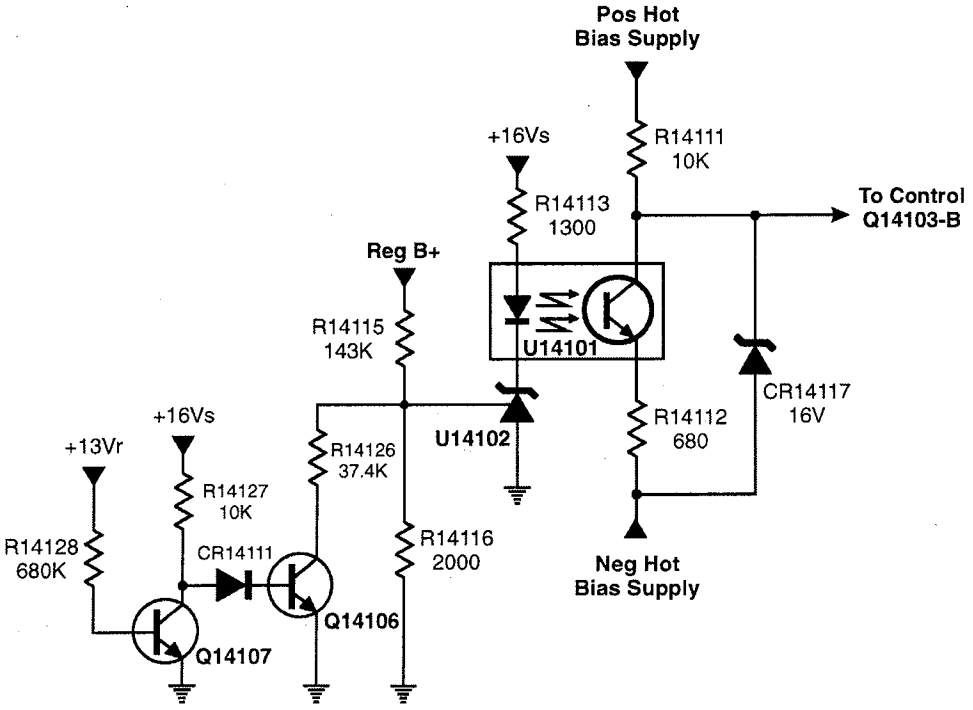


Figure 2-16, Run Mode

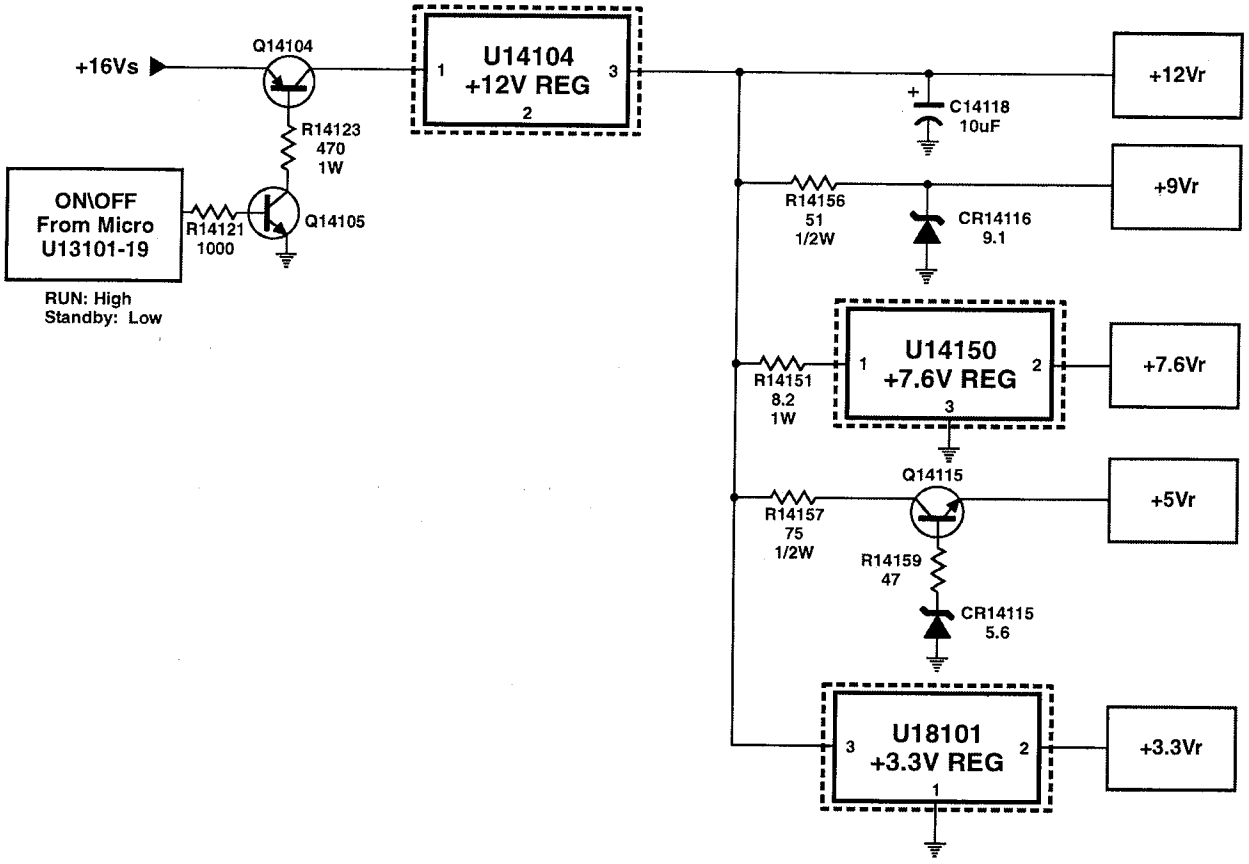


Figure 2-17, Run Supplies

Run Supplies

There are several supplies generated from the main supply but only required during run operation. They are shown in figure 2-17. To turn them on and off System Control sends a high to Q14105-B turning it on. That turns Q14104 on passing the +16Vs supply to the input of the main +12V regulator. The output of the regulator then feeds +12V directly to the circuits or feeds other regulators.

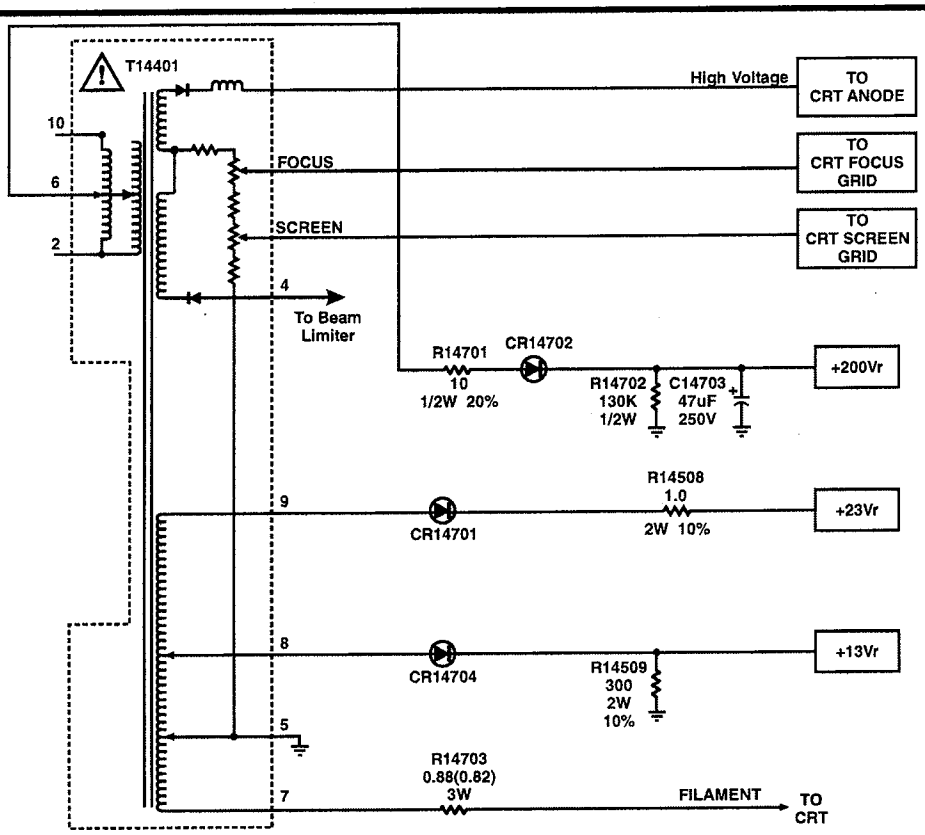


Figure 2-18, Scan Derived Supplies

Scan Derived Supplies

Several other sources of power must also be generated by the CTC203. They are derived from the scan circuits in a traditional way. Horizontal scan operation will be covered later.

Two low voltage supplies are generated; +23V and +13V. An AC filament supply for the CRT is taken from the same winding.

The CRT drivers require a higher voltage than can be generated by the normal supply. It is generated here and is about +200V. It is slightly unique as it is derived from the primary windings of the horizontal output transformer, not the secondary.

The remainder of the scan derived supplies are used to power and control the CRT. They are the anode, focus grid and the screen grid supply.

When output MOSFET Q14101 fails, it is a good idea to replace the latch transistors, Q14102 & Q14103. Unexpected excessive current may damage these transistors and other components in the immediate area.

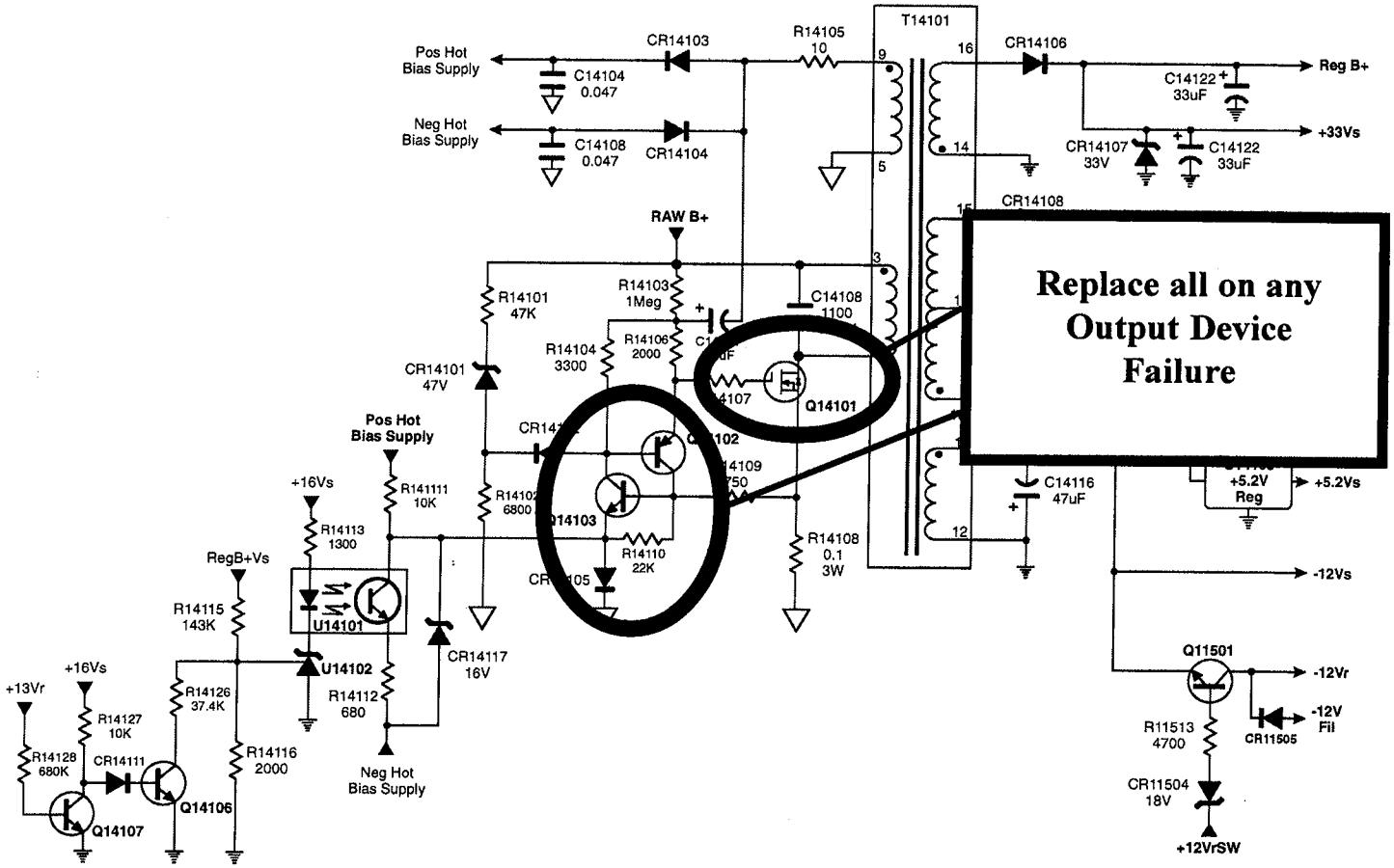


Figure 2-19, Main Power Supply (Repeated)

Deflection Overview

The CTC203 deflection circuits are very similar to previous TCE core line chassis. Some models will have pin-corrected yokes, while others use an active pincushion correction circuit. XRP is the same as previous chassis and other CRT control and protection is also similar.

The horizontal deflection system has two primary functions in the CTC203 chassis. First, it supplies the current for the horizontal yoke coils providing energy necessary to move the electron beam horizontally across the face of the picture tube. Second, it provides a number of voltage supplies needed for operation of the CRT and deflection.

Horizontal yoke current is provided by a circuit consisting of a switch (HOT), the primary inductance of the Integrated High Voltage Transformer (IHVT), a retrace capacitor, trace capacitor (S-Shaping capacitor), and the horizontal yoke coils.

Voltage supplies provided by the horizontal deflection system are derived from secondary and tertiary windings on the IHVT. The supplies are used by the video amplifier (kine drivers), tuner, CRT, and the vertical amplifier.

Low level signal processing circuits for the horizontal deflection system are contained in the T4-Chip. These include the horizontal sync separator and a two-loop horizontal AFPC system. The T4-Chip allows bus control of several parameters associated with the horizontal deflection system. These include horizontal drive pulse width, AFC Gain, Sync Kill, and ON/OFF.

Enabling or disabling the horizontal drive signal from the T4-Chip determines whether the chassis operates in the Standby or Run mode. In the Standby mode, no IHVT-derived supplies are present reducing standby power requirements.

The vertical deflection circuit in the CTC203 is a linear amplifier DC coupled to the vertical yoke coils. The circuit is similar to the CTC197 vertical circuitry. The vertical ramp is generated in the T4-Chip. Vertical size, bias, S-Correction, and linearity adjustments are done in the T4-Chip via the IIC bus. Timing information for the ramp generator is derived from a digital vertical countdown circuit, resulting in excellent interlace performance. The vertical output stage includes an integrated circuit containing the power amplifier, vertical flyback generator, and thermal protection.

Deflection Basics

This discussion will only touch on horizontal, (right-left, left-right) deflection of the electron beam across the face of the CRT. Vertical, (up/down, down/up), deflection occurs in a similar fashion, just a different direction on the screen.

Although there is only one horizontal yoke winding, it is wound in such a fashion that current in one direction drives the beam away from center to the left side of the screen, while current in the opposite direction drives the beam away from center to the right side of the screen. The strength of the current determines how far from the center the beam is deflected.

Deflection is accomplished by forcing current through the deflection yoke, creating an electromagnet from the yoke windings that either push the electron beam away from or allow it to drift back to the center of the screen. If there is no yoke current, the beam remains center screen creating a vertical line very close to the physical center of the CRT. Figure 3-1 and 3-2 show the electron beam position at various yoke current values, assuming a static DC current from a power supply is used. (These values are only for discussion and demonstration purposes. Actual yoke current and direction for exact beam positioning will be different.) Note that as yoke current increases towards a higher positive value, the beam is driven farther towards the right side of the screen. As the positive yoke current approaches zero, the beam is closer and closer to center screen.

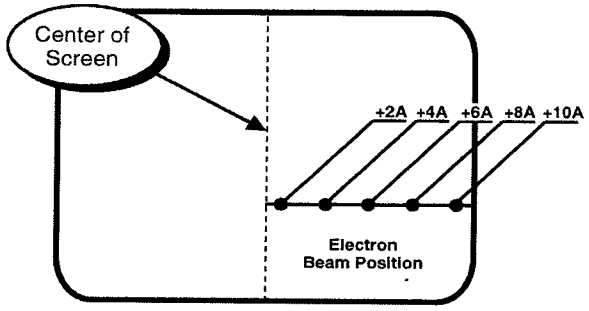


Figure 3-1, Electron Beam Position with Positive Current

As yoke current reverses, the beam is again driven away from center screen, but now in the opposite direction. The higher the negative current, the farther from center screen the beam is driven. As negative current decreases, the beam moves back towards center screen.

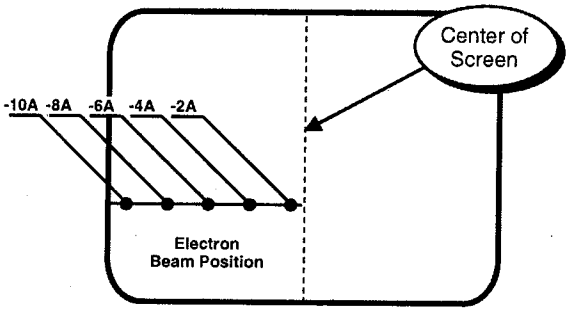


Figure 3-2, Electron Beam Position with Negative Current

Figure 3-3 shows how increasing positive current drives the electron beam towards the right side of the screen and increasing negative current drives the beam towards the left side. The amplitude of current drives the beam farther from center screen. (The scope captures are not in exact time alignment with the electron beam.)

Again, the theory of positive and negative current flow is not important to this discussion. The concept of yoke current flow one way making the beam travel one direction, while yoke current flow in the *opposite* direction makes the beam *reverse* its travel is the point.

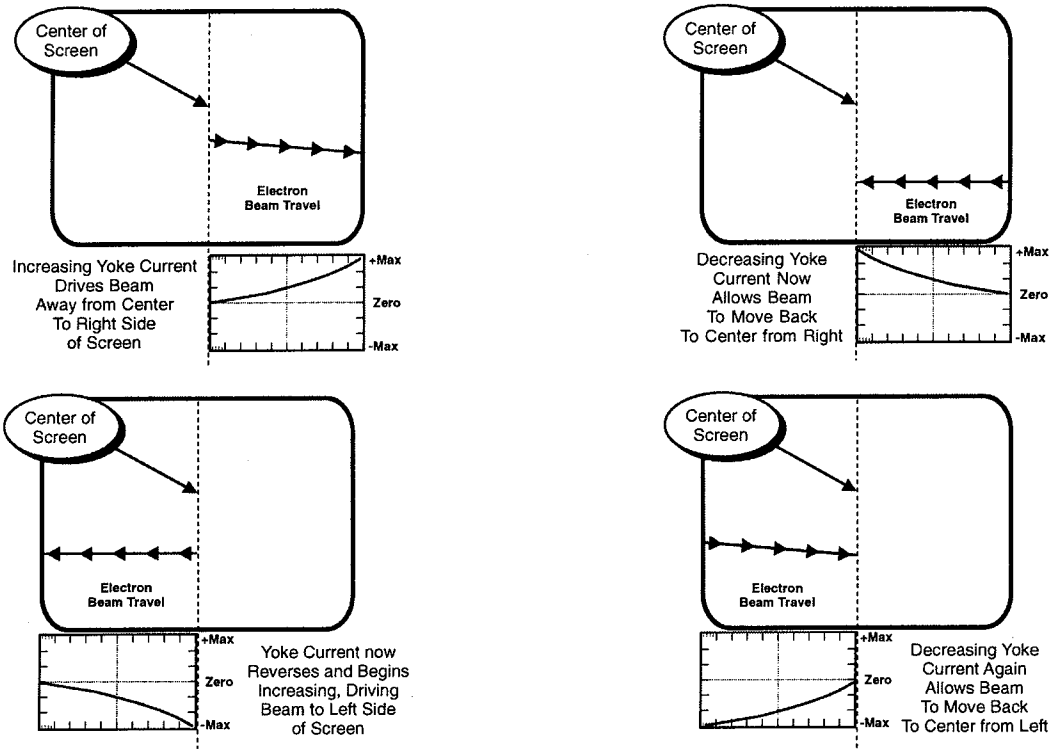
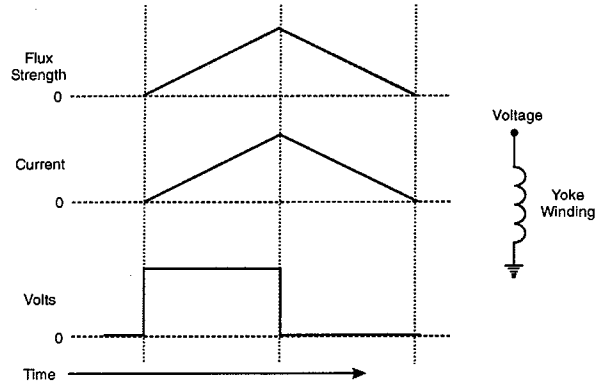


Figure 3-3, Beam Travel

Inductive Current Flow

Among the many theories of deflection, yoke current versus yoke voltage is one of the most misunderstood by technicians. A yoke is simply an inductor constructed to induce its developed magnetic flux in a specific pattern around the bell of a CRT. The flux becomes stronger as current through the wire is increased, and weaker as it decreases. Figure 3-4 compares voltage across a yoke winding with the resulting current through it and magnetic field developed by it.

As voltage is first applied, the yoke tends to "limit" current flow. Even though maximum voltage is immediately available, current builds slower as a result of inductive reactance. As current builds, magnetic flux fields emanating from the yoke grow stronger.



When voltage is removed, the yoke tends to continue current flow as the flux fields (with no current flow to sustain them) begin to collapse. As they collapse, current decreases and the magnetic field grows weaker. If voltage is not reapplied, the current will fall to zero. The yoke is not directional. If the opposite polarity voltage is applied, the same current pattern is observed, only in the opposite direction.

Figure 3-4, Yoke Current versus Applied Voltage

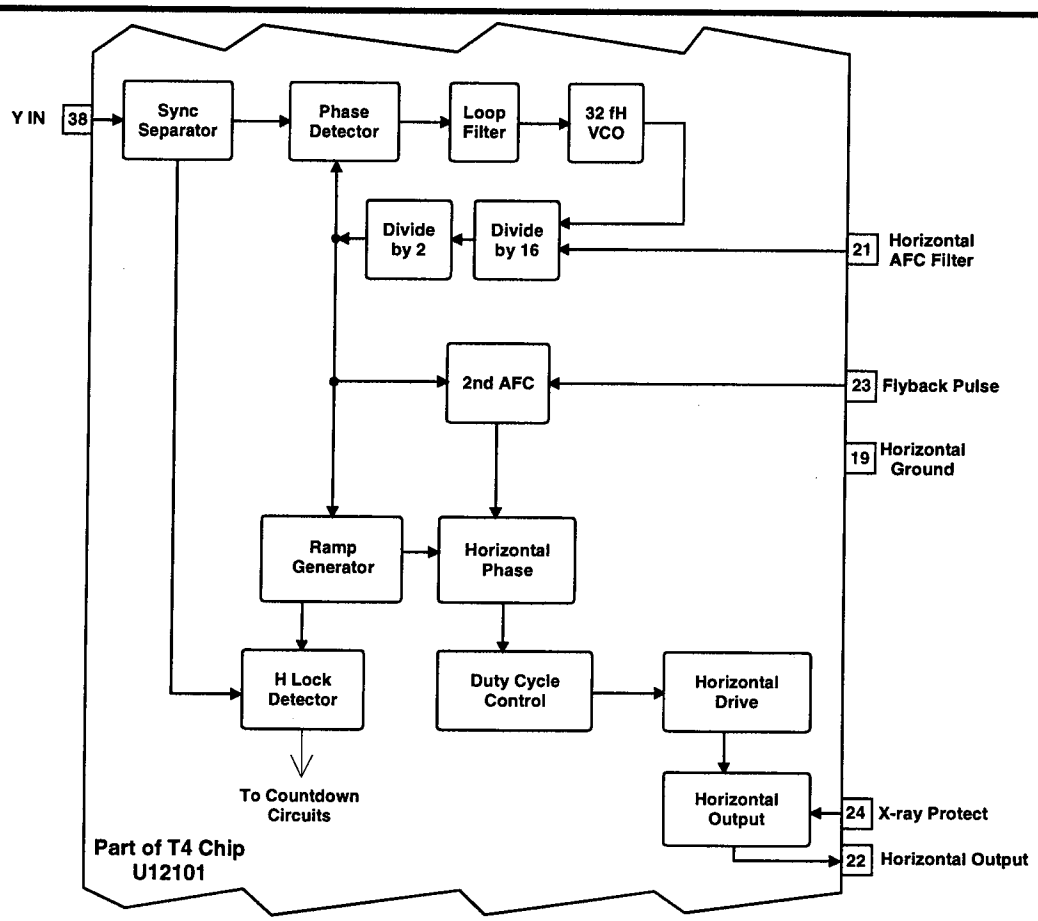


Figure 3-5, T4-Chip Horizontal Deflection

Low Level Horizontal Deflection

The T4-Chip employs a two loop horizontal AFC system. The first loop is used to lock an internal 1H clock to the incoming horizontal sync signal derived from the baseband luma signal. The second loop is used to lock the 1H clock to a feedback pulse derived from a secondary winding on the IHVT. As with the other T-Chip versions, a horizontal to video phase control is available via the IIC bus. The phase control can be used as a horizontal centering control during alignment.

The first loop employs a 32H (32 times the horizontal frequency) VCO referenced to a 503 kHz ceramic resonator.

The output at U12101-22 is shown.

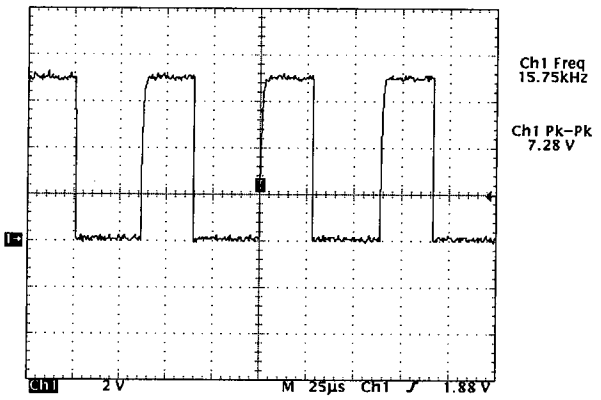


Figure 3-6, U12101-22 Output Waveform

Low Level Signal Generation

The low level horizontal waveform generated from the T4-Chip has all correction signals added prior to the output from U12101-22.

The horizontal driver circuit serves as an interface between the low level horizontal output of the T4-Chip and the high power horizontal output circuit. The driver operates in a "flyback" configuration storing energy driver transformer, T14301, during the conduction cycle of Q14301. When Q14301 turns off, stored energy is dumped into the base of Q14401, the horizontal output transistor (HOT). A buffer stage has been added to reduce the amount of current that must be handled by the T4-Chip horizontal output stage. This buffer consists of Q14302 and its associated circuitry.

The horizontal drive waveform appearing on T14301-6 is shown.

A sample of the flyback pulse is taken from the filament winding and fed back to the T4-Chip. This pulse provides a feedback signal to ensure horizontal stability.

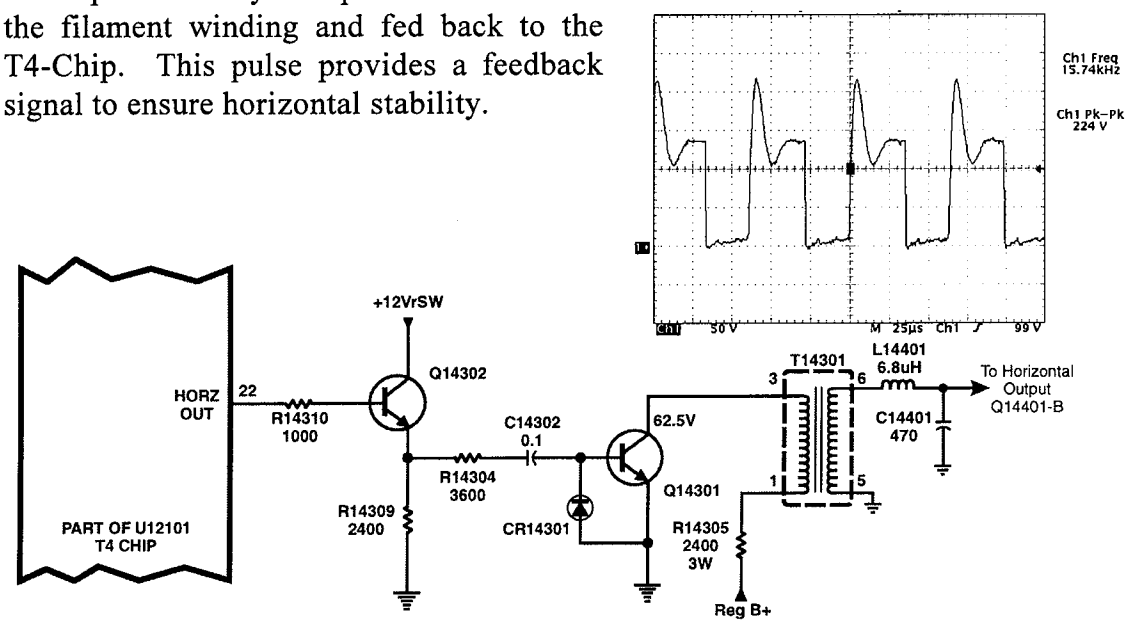
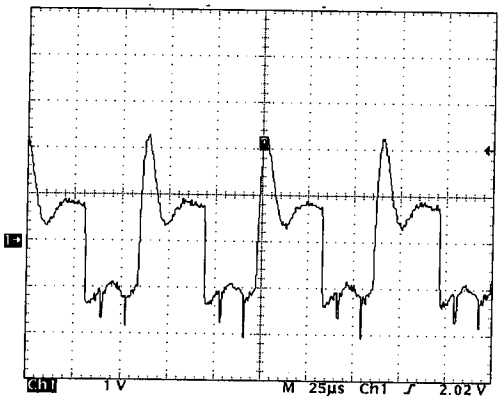


Figure 3-7, Low Level Horizontal Signal Generation

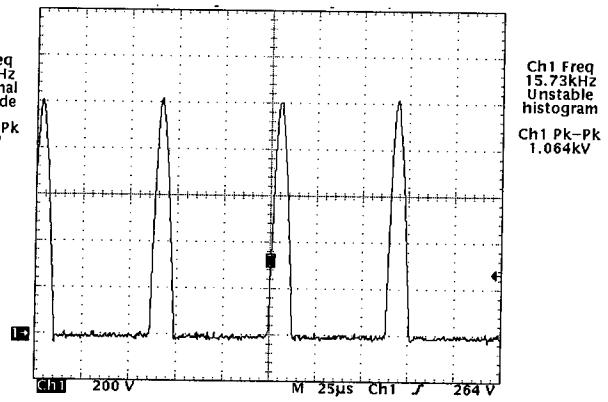
Horizontal Output

The horizontal output circuit generates a high current ramp waveform used to drive the horizontal yoke. It also drives the high voltage transformer (IHVT), producing supplies necessary for CRT operation. These supplies include the anode supply (high voltage), focus and screen grid supplies, cathode B+ (Kine drive), and filament voltage. Additional secondary supplies are provided for the vertical amplifier.

Figure 3-8 shows a simplified diagram of the horizontal scan circuit and several waveforms during normal operation. The first waveform is the output of the horizontal drive transformer, T14301-6. The next waveform is the output at Q14401-C. Flyback voltage required to return the electron beam is much greater than scan voltage, generally reaching about 1000V!



T14301-6



Q14401-C Retrace

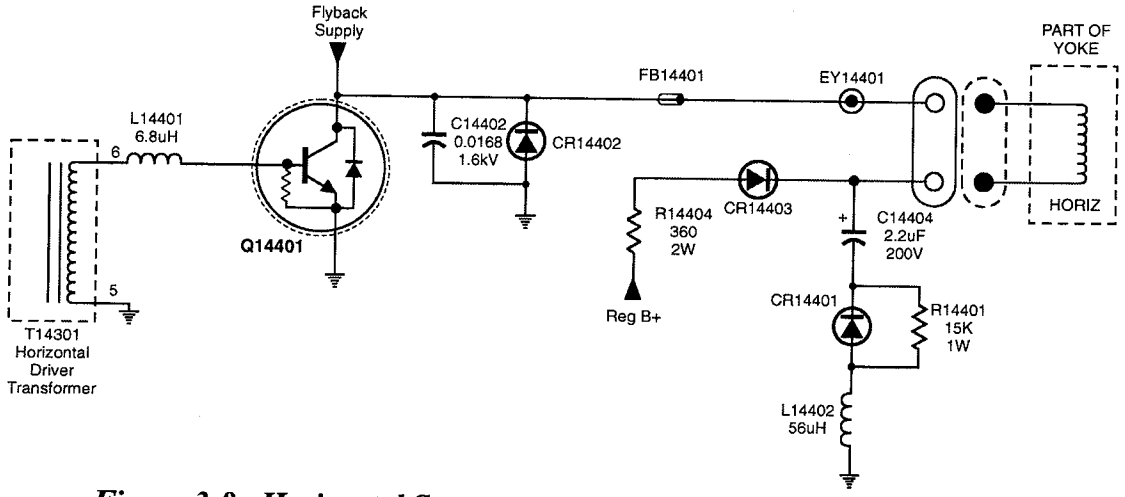
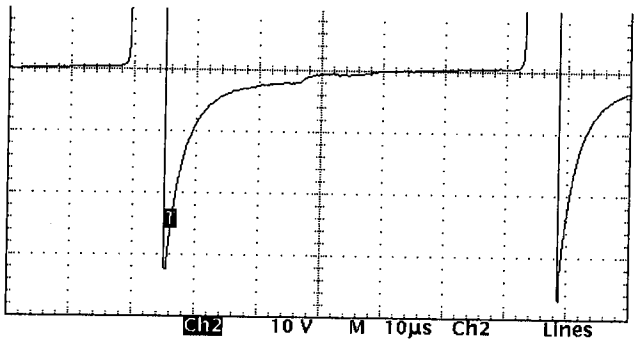


Figure 3-8, Horizontal Scan

This is an expanded waveform from Q14401-C showing the trace portion of the horizontal output (*Q14401-C Trace*). The retrace pulse (*Q14401-C Retrace*) is easy to see, but what happens to the waveform during trace is unlikely to be caught on a normal analog or digital scope. The bottom waveform is expanded and represents active trace. In Figure *Q14401-C Retrace*, active trace appears to be a flat voltage, while Figure *Q14401-C Trace* reveals the true waveform.



Q14401-C Trace

Horizontal Scan Operation

In any discussion of deflection circuits, actual current flow and voltage diagrams prove to be of little use. It is more important to understand energy flow during trace and retrace periods. By understanding how and when energy is transferred troubleshooting becomes more routine. The CTC203 uses a fairly common configuration for horizontal scan and high voltage generation, however, without understanding the energy transfer, troubleshooting efforts may be reduced to "shotgunning" parts.

The technician must realize with no yoke current, the electron beam would rest in the middle of the screen. Remember, yoke current deflects the electron beam from center screen one direction with positive current flow and the opposite direction with negative current flow. The amplitude of the current determines how far deflection pushes the beam from center. Decaying amplitude allows the beam to return to center screen.

Although Figure 3-9 shows the major components of horizontal scan, the interaction of scan and the high voltage generation portion of the horizontal output section is critical. The high flyback voltage necessary to return the electron beam to the left side of the screen is a product of the high voltage generator as is CRT beam control and generation.

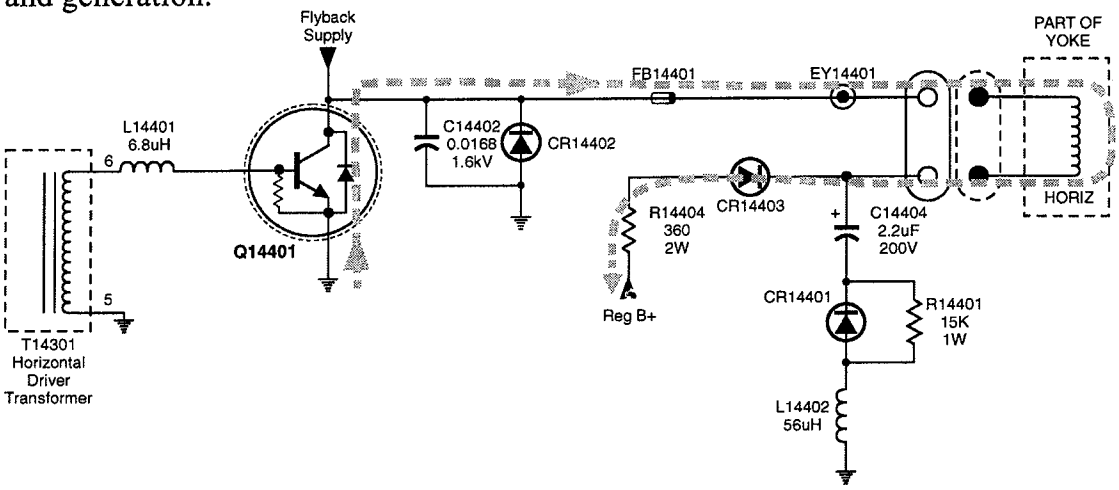


Figure 3-9, Beginning of Horizontal Scan, Trace Center to Right Screen

When scan begins Q14401 is turned on. Current now begins flowing through the yoke in a path from ground through Q14401, the yoke, CR14403 and R14404 to Reg B+. At the same time, the S-Cap, C14404 is charging to Reg B+ through R14401 and the linearity coil, L14402. When the beam reaches the extreme right side of the screen, yoke current is at a maximum in the positive direction, trace is finished and the input waveform shuts off Q14401.

Now a high voltage generated from the IHVT, (the flyback voltage shown previously) is placed on Q14401-C. Two things happen. First, current in the yoke begins to decay rapidly without a source and the beam begins to deflect in the negative (right to left) direction. Yoke current is dumped into the retrace capacitor, C14402 during the buildup of the flyback voltage. The retrace capacitor forms a resonant circuit with the yoke. At the same time, flyback voltage has reached a peak and is also dumping energy into the retrace capacitor charging it to an extremely high voltage. As yoke energy reaches zero, current flow is also zero and the electron beam is at center screen.

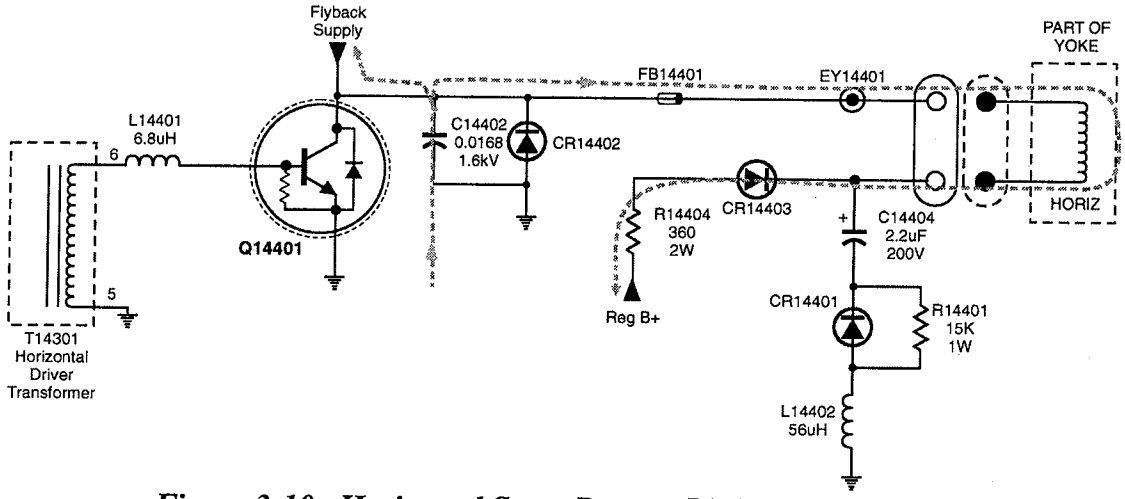


Figure 3-10, Horizontal Scan, Retrace Right to Center Screen

Flyback supply energy is now decreasing rapidly and the voltage at Q14401-C drops. The second half of retrace, from center screen to the far left occurs when the flyback supply energy just stored in the retrace capacitor resonates with the yoke. The difference now is current flow direction. Yoke current now begins building in the *opposite* direction causing the beam to deflect from center screen to left.

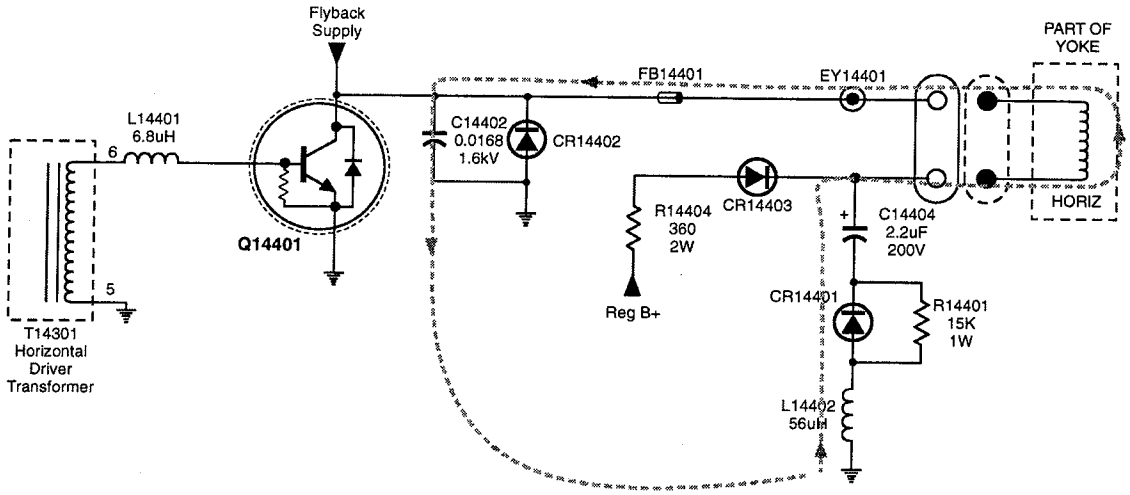


Figure 3-11, Horizontal Scan, Retrace Center Screen to Left

TECH TIP

At the moment the retrace capacitor has delivered all its energy to the yoke, Q14401-C voltage is about zero. If any energy is still in the flyback supply it could cause raster distortion or catastrophic failure of horizontal output components. At this point the damper diode, CR14402 begins to conduct, diverting this energy away from the yoke and other components and starting trace.

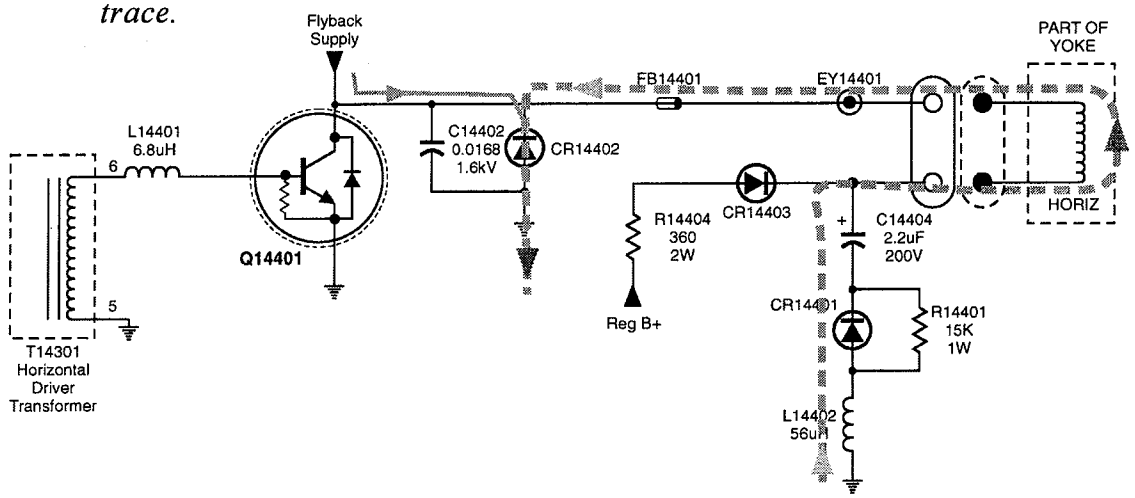
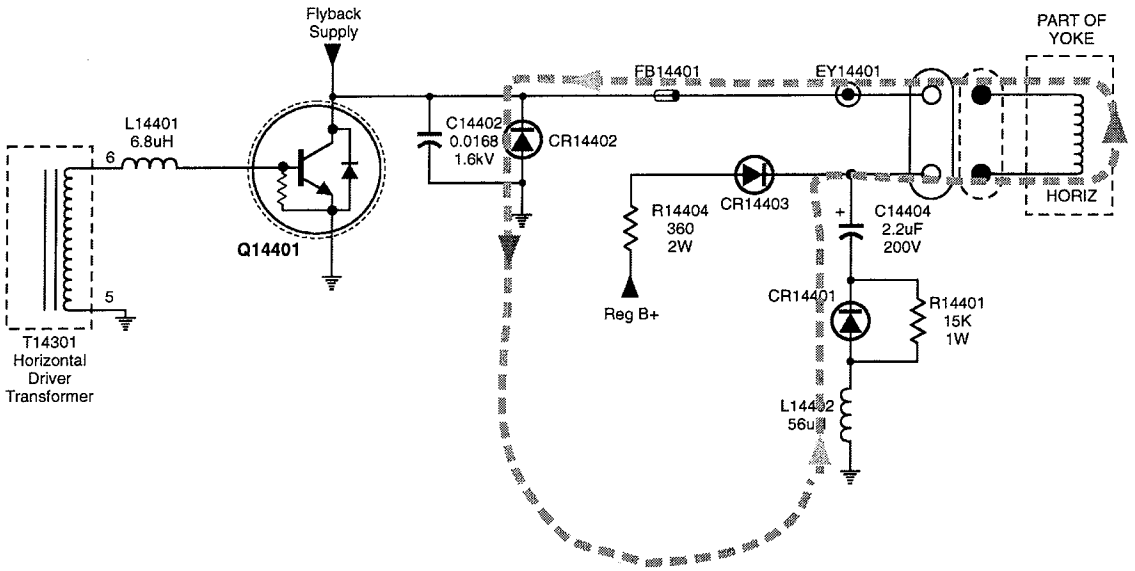


Figure 3-12, Horizontal Scan, Damper Diode

Figure 3-13, Horizontal Scan, Trace Left to Center



Yoke energy is now maximum keeping the beam on the left side of the screen. The beginning of trace (electron beam moving from left to center screen) occurs as yoke current begins to flow through the damper diode and S-Cap, C14404. Yoke energy now decreases with decreasing current and the beam moves from left to center screen. The S-Cap is now controlling how fast energy is lost from the yoke, thus controlling how fast the beam is moving.

As the trace reaches center screen, the incoming horizontal waveform turns on Q14401. Reg B+ is now applied to the yoke and the scan cycle begins again starting from center screen to right.

Horizontal Pincushion

Horizontal pincushion correction is used to compensate for horizontal scanning distortion that occurs as a function of vertical position.

The horizontal output circuit contains provisions for geometry correction including linearity correction, S-correction, and EW pincushion correction. Linearity correction is provided by the linearity coil, L14402. A parallel damping network consisting of C14405 and R14403 are included to reduce ringing in the coil at the beginning of scan. S-correction is achieved by the S-capacitor, C14404.

East-West pincushion correction is handled differently by the CTC203 depending on the size of the CRT. Screen sizes smaller than 27" have pin corrected yokes and require only some tweaking of components to accomplish pin correction. In VLS (Very Large Screen) CRT's East-West pin correction is done by a diode modulator circuit. The diode modulator is a 'pseudo" horizontal circuit operating under the normal horizontal output.

Figure 3-14 shows a simplified schematic illustrating the principle of the diode modulator. An active pin correction circuit buffering an E/W control waveform from the T4-Chip, U12101-17, controls the voltage at the junction of L14801 and C14805. Since the amount of horizontal scan is proportional to the voltage across the S-capacitor, C14404, the pin circuit can control the amount of scan by controlling the voltage at the bottom of C14404. The voltage at the top of C14404 is essentially held at reg B+. To achieve pin correction, a vertical rate parabolic waveform is produced by the pin circuit and applied to the S-capacitor. This produces the desired modulation of horizontal scan. Another feature of the diode modulator is that it allows width adjustment. This is also achieved by varying the dc voltage at the bottom of the S-capacitor.

Typical pincushion problems would be either not enough correction or too much. This would be seen as the correction waveform amplitude too low or too high. Too much amplitude or failure of the pin correction circuit would result in a noticable pincushion distortion of the raster. Too little amplitude would result in barrel distortion.

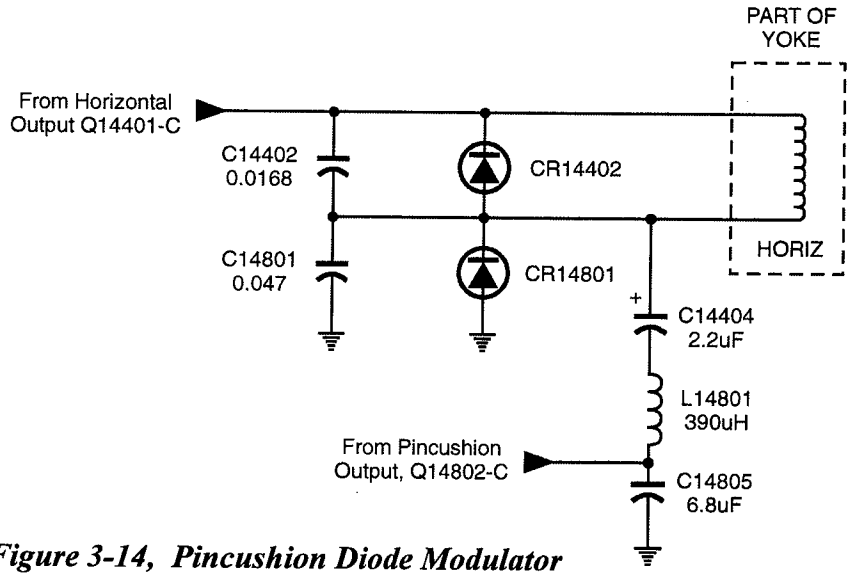


Figure 3-14, Pincushion Diode Modulator

XRP

The X-Ray Protection (XRP) circuit shuts down the horizontal deflection in the event of a detected fault if that fault induces CRT radiation exceeding acceptable limits. The circuit produces a DC voltage which is proportional to the CRT anode voltage. This voltage is compared to a bandgap reference within the T4-Chip. If the detected voltage exceeds the internal reference, a latch is set which shuts down the horizontal drive output from the T4-Chip. This, in turn, disables the anode voltage shutting down the CRT.

The XRP latch in the T4-Chip can only be reset via the IIC bus with an on to off transition of the T4-Chip On/Off register. This allows software controlled restarts after nuisance XRP trips.

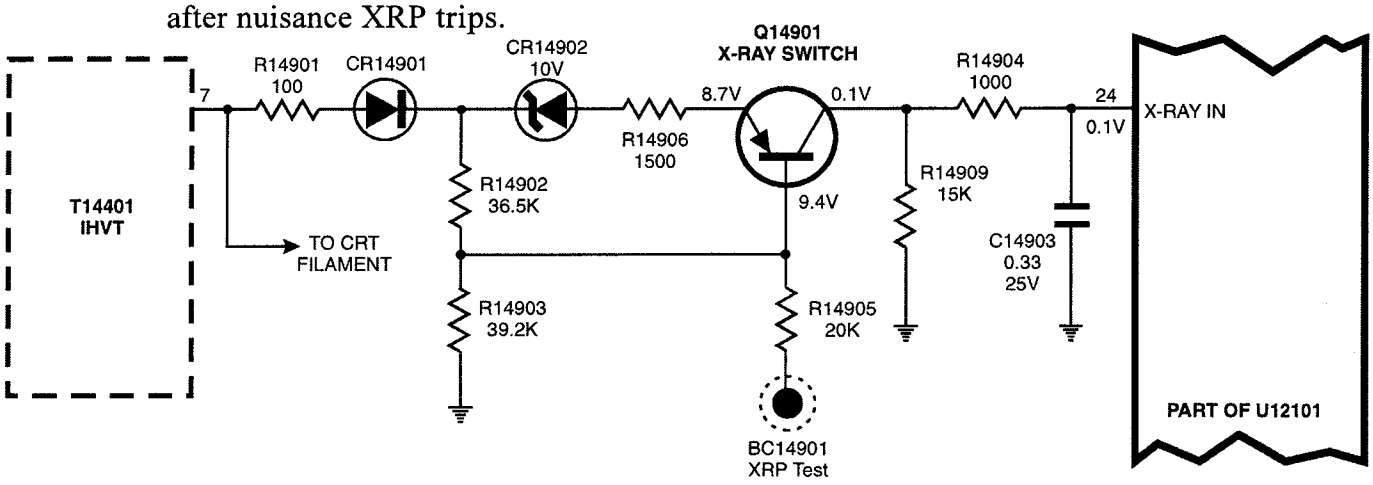


Figure 3-15, XRP

The heart of XRP circuit is in the T4-Chip. U12101-24 is the input to the XRP comparator. This comparator has a reference voltage of +3V ±12mV (4%). The reference voltage is produced by a temperature stable bandgap reference. If the voltage at the input exceeds the 3 volt reference, a latch is set which inhibits horizontal output from the T4-Chip. This action defeats the ability of the chassis to produce high voltage, eliminating a possible x-ray threat.

The XRP detector voltage is produced by the filament winding of the IHVT from pin 7. This output is designed to closely track high voltage. The filament voltage is peak detected by CR14901, producing a DC voltage proportional to the high voltage. The DC voltage is applied to a precision resistor divider consisting of R14902 and R14903. Values of the XRP divider are chosen to produce correct XRP trip thresholds for each CRT. If the voltage becomes large enough, zener diode CR14902 breaks over, and Q14901 turns on. Current flows through R14909 and begins to drop voltage proportionally. When the current increases enough, the voltage on U12101-24 will exceed the 3 volt level of the XRP comparator in the T4-Chip and the XRP latch is set.

For a typical XRP trip, System Control will try to restart horizontal after a time delay of about 1.5 seconds. If there are three of these attempted restarts within one minute, the chassis will shut down. At this point it will be necessary to turn the set back on via the front panel or the remote.

Z-Axis Correction

The Z-Axis correction circuit is used to counteract raster rotation when the picture tube is oriented in a north or south direction. This is accomplished by adding a DC magnetic field to counteract the Earth's magnetic field.

The CTC203 will use a microprocessor controlled approach to Z-Axis correction previously used in the CTC197 chassis.

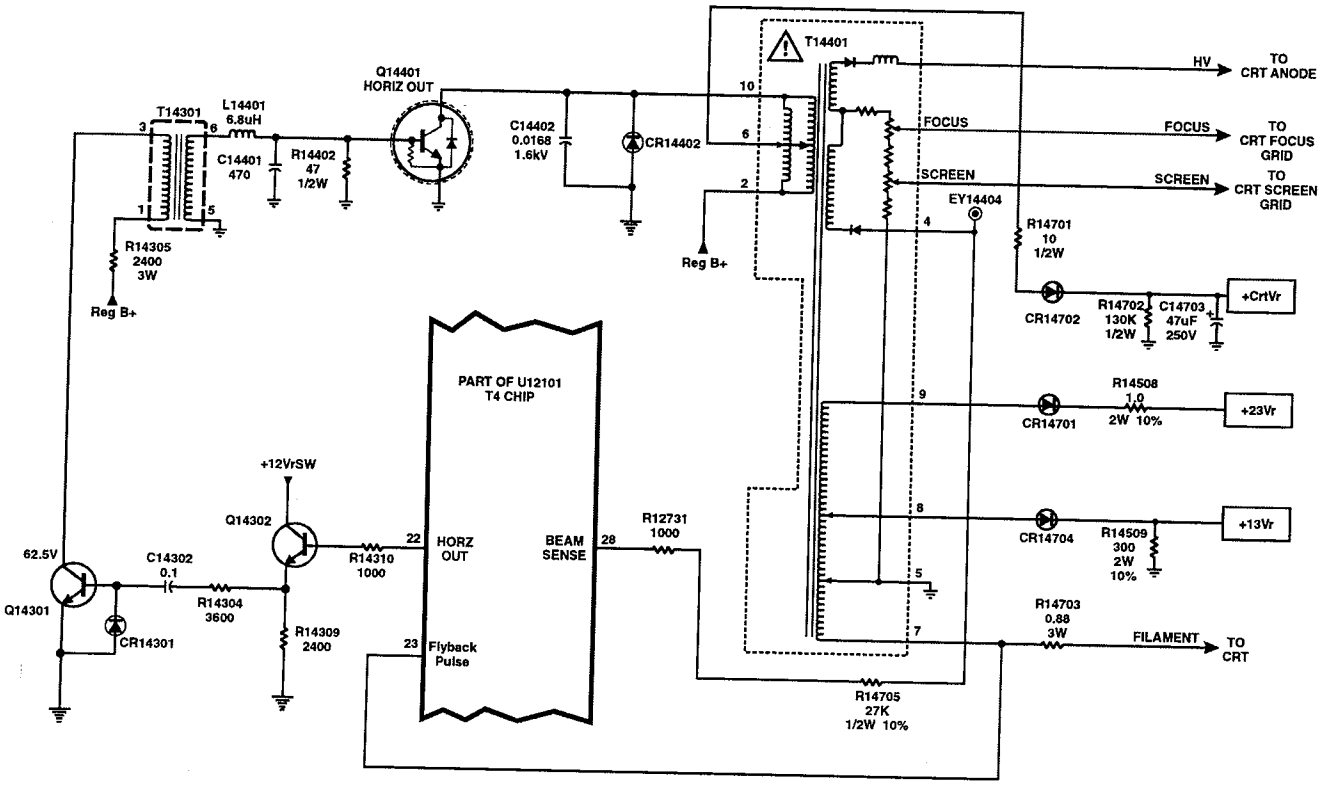


Figure 3-16, Scan Derived Supply Generation

Horizontal Scan Derived Supply Generation

The scan derived supplies covered in the power supply section are shown again here. The horizontal output transistor, Q14401 supplies the current demands of these supplies and also horizontal deflection.

In this configuration, the horizontal yoke windings are connected in parallel with the primary windings of the IHVT, T14401. During retrace the combined flux energy in the yoke and IHVT primary winding is being dumped into the retrace capacitor, C14402. T14401 voltage across the primary reaches a maximum, greater than +1000V and quickly decreases as it transfers energy to the retrace capacitor. If the retrace capacitor changes value, raster width is directly affected, but so is the resonance between it, T14401 and the horizontal yoke winding. Energy transfer decreases, peak current is not reached and excessive heat dissipation in the horizontal output circuits will result.

Two samples of the secondary voltages are fed back to the T4-Chip. One is a sample of the filament supply used to lock the output frequency to the input. The second is a sample of the current generated in the secondary winding supplying anode and grid voltages. Since the anode supply also supplies beam current, this may be used to monitor the CRT electron beam. If beam current increases too much, CRT drive may be reduced in the T4-Chip, reducing beam current.

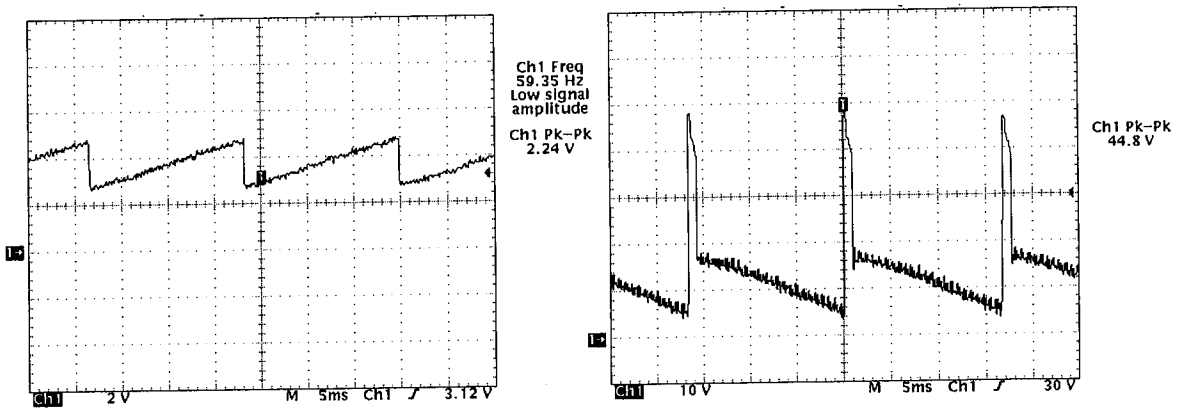
Vertical Scan Overview

The vertical deflection circuit in the CTC203 is a single IC, linear amplifier DC coupled to the vertical yoke coils. The vertical ramp is generated in the T4-Chip. Vertical size, bias, S-Correction, and linearity adjustments are done in the T4-Chip via the IIC bus. Timing information for the ramp generator is derived from a digital vertical countdown circuit. This results in excellent interlace performance. The vertical output stage includes an integrated circuit containing the power amplifier, the flyback generator, and thermal protection.

The vertical circuit in the CTC203 is very similar to the CTC197, CTC179/189 and the earlier CTC177 vertical circuits. Like the earlier chassis, the output amplifier is DC coupled instead of capacitively AC coupled. The DC coupled circuit has the advantages of fewer parts, lower cost and linearity becomes less dependent on electrolytic capacitor tolerance and aging. "S" correction, the tendency of the horizontal lines to be spaced closer at different points in the screen, is accomplished inside the T4-Chip.

Because of DC coupling, the DC level of the vertical reference ramp from U12101-15 affects vertical centering. This allows vertical DC (vertical centering) to be included in the digital alignments. By moving the vertical ramp higher or lower around a DC voltage, vertical centering is accomplished. This also compensates for tolerances in the reference ramp DC voltage.

The vertical circuit acts as a voltage to current converter. It changes the vertical rate DC ramp signal out of the T4-Chip to a current ramp through the yoke deflecting the electron beam from top to bottom and bottom to top on the CRT. Figures 3-17 and 3-18 show the vertical circuits and a typical output waveform from the T4-Chip, U12101-15 and the resulting output from vertical IC, U14501-5. The vertical output IC, U14501, is an inverting amplifier that sinks current at pin 5 when pin 1 is high and sources current from pin 5 when pin 1 is low. U14501 is supplied by the +23 volt run source from the horizontal scan-derived run supply.



U12101-15 U114501-5

Figure 3-17, Vertical Waveforms

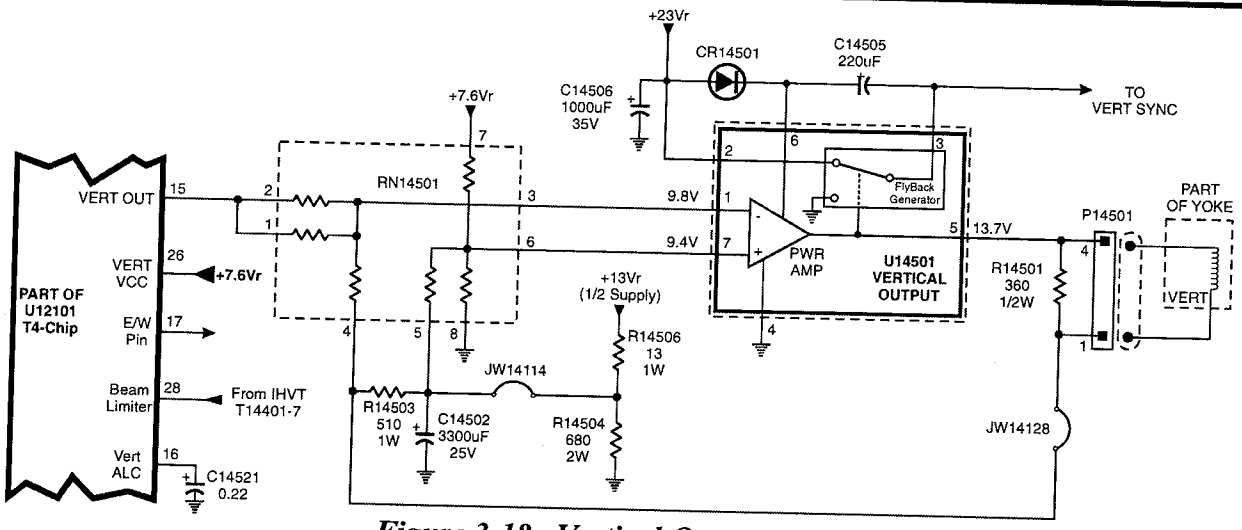


Figure 3-18, Vertical Output

Half-Supply

An important aspect of the vertical circuitry is the "half supply". It is connected to the low side of the yoke and remains at approximately half of the +26 volt supply. The supply is developed from a secondary winding of the IHVT and CR14704. The +26 volt supply is taken from a portion of the same winding which means the +26 volt and the +13 volt supply track each other. The purpose of the half supply is to provide a reference voltage to the vertical circuitry, around which yoke current is generated.

In discussions on horizontal scan it was noted that without yoke current, the electron beam would stay at center screen. The vertical yoke windings are similar except deflection occurs in from top to bottom and bottom to top. Current in one direction deflects the beam up. Current in the opposite direction deflects the beam down. Current through the yoke must travel in two directions to accomplish one complete scan of the CRT screen.

Scan begins from center screen (zero deflection current) and travels downward. If there is no input to U14501, output voltage on pin 5 is about 1/2 the supply or around +13V. With the top and bottom of the vertical yoke winding at +13V, there is no yoke current and the beam is at center screen. The vertical waveform on the input of U14501 is positive going at this point. Since the amplifier inverts, the output is negative going (towards ground). The output is connected to the top of the yoke which means it is also negative going during this time. Since the half-supply is connected to the bottom of the yoke, when pin goes to zero volts, there is about 13 volts of potential across the yoke winding but in the negative direction.

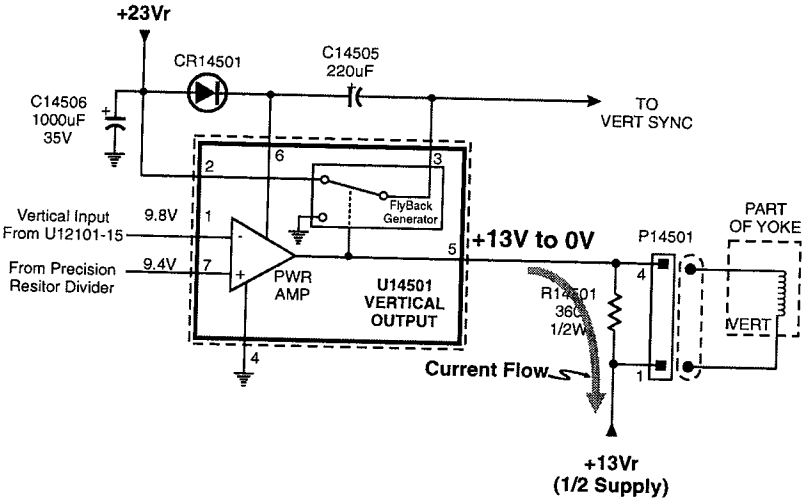


Figure 3-19, Vertical Scan from Center Screen to Bottom

When retrace begins, the flyback supply (more on this supply later) is placed on the output of U14501. The flyback supply is about +43V which is now on the top of the yoke. Since the bottom of the yoke is still connected to the flyback supply, there is now about +30V (+43V – +13V) across the vertical yoke winding. Current in the yoke decreases rapidly from a maximum negative towards a positive flow. It first allows the electron beam to travel back to center screen as it decreases, then causes current in the opposite direction and the electron beam starts to travel rapidly from center screen to top.

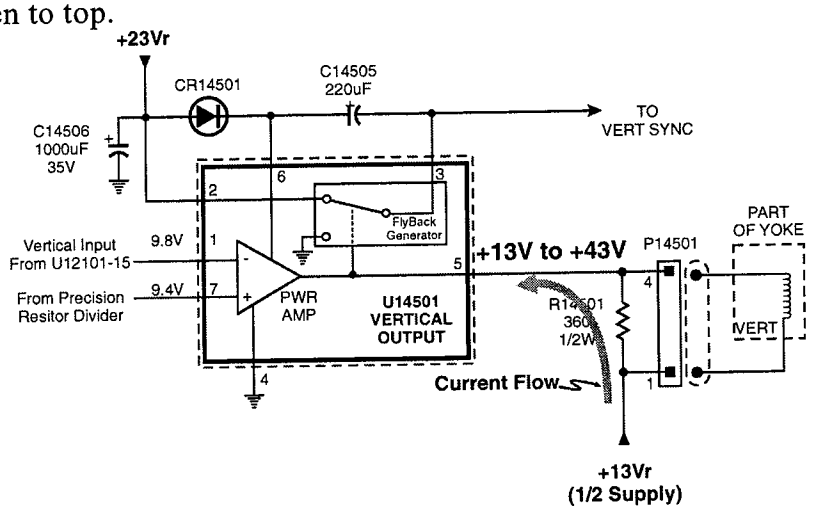


Figure 3-20, Vertical Scan from Bottom to Top

As the beam reaches the top, scan begins again, with the input waveform now driving the output towards zero (ground). First, the maximum positive current flow decreases to zero allowing the beam to go from the top of the screen to center. Then the negative current flow portion of scan from center to bottom begins as U14501-5 drops below +13V and towards zero. Scan now begins again.

The resistors on pins 7 & 8 of RN14501 limit current in the yoke to keep the beam from deflecting off the screen in the event U14501 might short to ground or to the +26 volt source. C14502 acts as a filter and with R14504 helps reduce the vertical rate ripple current on the "half supply." The half supply is input to pin 5 of RN14501 and through R14503 to pin 4 of RN14501. The bias voltage at RN14501-5 goes out pin 6 to the vertical IC noninverted input at U14501-7. The bias voltage at RN14501-4 goes out pin 3 to the inverted input of the vertical IC, U14501-1. This helps to cancel any modulation of the half supply resulting from vertical rate current on C14502. The quality of the canceling effect is determined by the match of the resistors in RN14501. These are normally matched to within 0.5 percent.

U12101-15 provides a 2 volt p-p vertical sawtooth to pins 1 and 2 of RN14501. The average DC level of the ramp is approximately half the T4-Chip vertical supply voltage (7.6V) on pin 26 (approximately 3.81 Vdc). The ramp can be adjusted ±150mV via the Vertical DC Centering adjustment over the IIC data bus using either the front panel service menu or Chipper Check. The vertical ramp and error signal superimposed on the half supply from the current sense resistor, R14503, are added together by the resistor network, RN14501, and input to the inverting input pin 1 of U14501. The +7.6 volt supply is input to pin 7 of RN14501 where it is divided

down to half Vcc. It is then added to the error signal riding on the half supply from the current sense resistor, output from pin 6 of RN14501 and applied to the non-inverting input pin 7 of U14501. The average DC voltage on pin 7 is about 9 volts during normal operation.

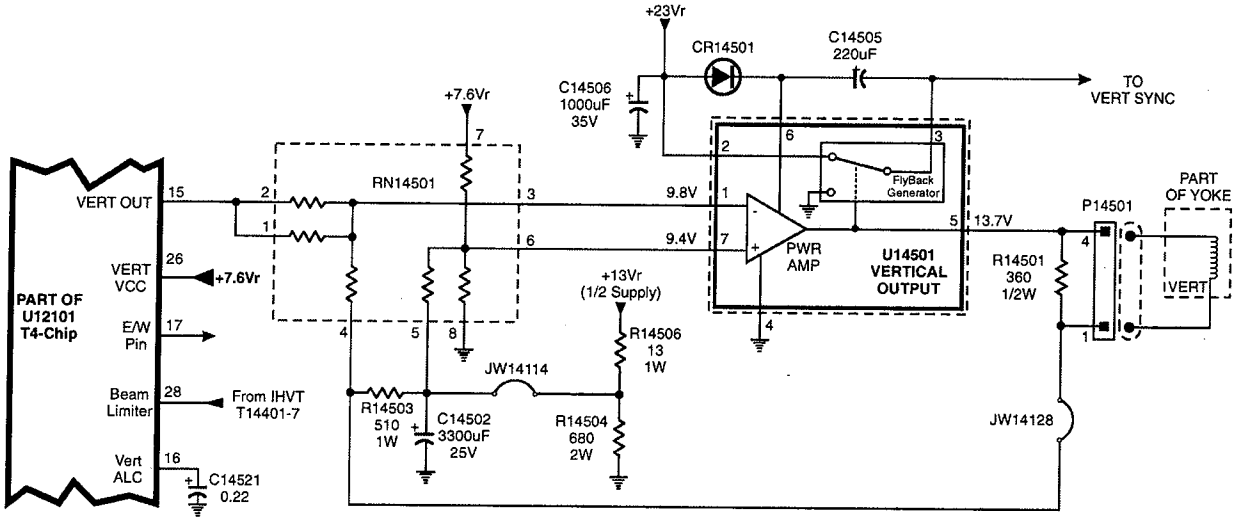


Figure 3-21, Vertical Output (Repeated)

Vertical Flyback Supply

During the active portion of scan, current flows in such a direction to cause the beam to travel down the face of the CRT. During retrace, the yoke must stop the downward travel of the beam and return it to the top of the screen by reversing the yoke current. The beam travels down the screen in 1/60th of second, but has to return to the top in much less time. The vertical circuitry uses some tricks to accomplish the task.

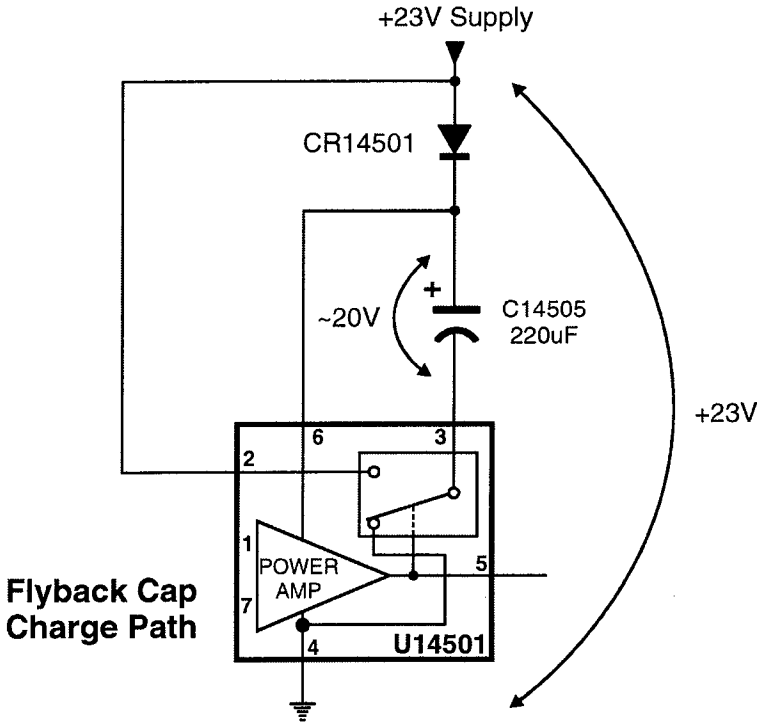


Figure 3-22, Vertical Flyback Supply Charge Path

During retrace, the ramp resets causing the output of U14501 at pin 5 to go high, deflecting the beam to the top of the screen. The extra current required to deflect the beam from the bottom to the top of the screen is produced by C14505. During scan time, the negative lead of C14505 is grounded by an internal relay through pin 3 of U14501 (Figure 3-22). The capacitor charges to about 20 volts.

At retrace, the flyback generator switch inside U14501 connects pin 3 to pin 2 (Figure 3-23) applying the +23 volt supply in series with the now charged C14505. The charge stored on C14505 plus the 20 volts on its negative terminal produce about +43V on pin 6, the positive power supply lead of U14501. The increased supply voltage quickly brings the beam to the top of the screen. Figure 3-24 shows a typical output waveform from U14501-6. Note the normal DC output level of +23V with the flyback voltage only being delivered during retrace.

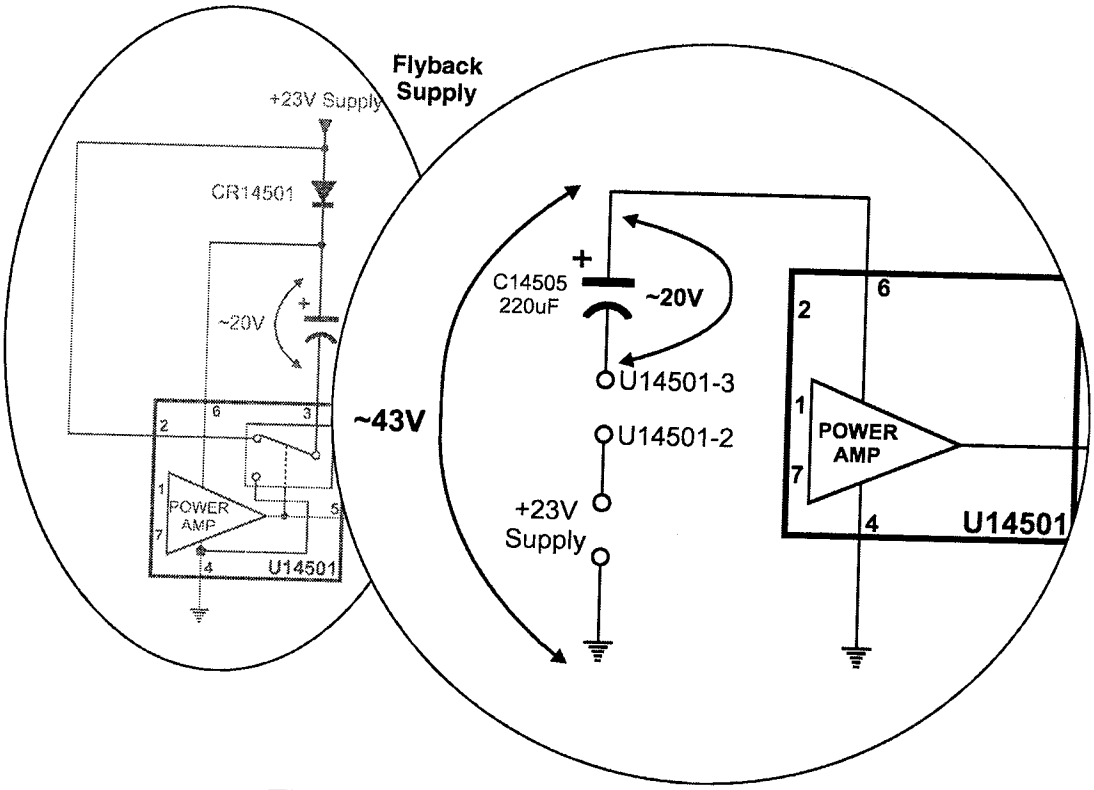


Figure 3-23, Vertical Flyback Supply

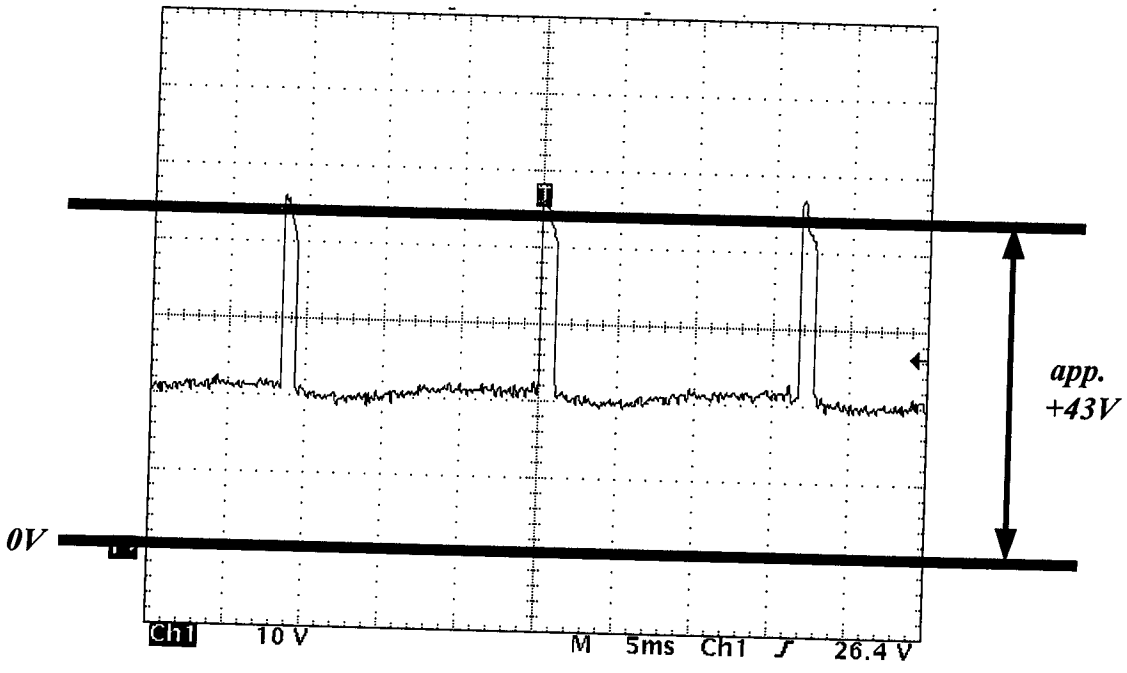


Figure 3-24, Vertical Flyback Waveform

Beam Limiting

There are several inputs and outputs from the T4-Chip related to vertical scan. Vertical size compensation with varying beam current is achieved via pin 28 of U12101. The vertical output ramp at U12101-15 will change about 1 percent per volt of change at pin 28. Pin 28 is nominally 6.1-7.3 volts during normal operation. As beam current increases toward the beam limiter threshold, a point is reached when the beam sense line will begin pulling down the voltage reference at pin 28. This causes a drop in the vertical reference ramp at U12101-15 reducing vertical scan slightly and preventing the raster from blooming vertically during high beam current video.

Vertical Ramp ALC

U12101-16 is the vertical ramp ALC (automatic level control) that maintains the vertical ramp at a constant level, even if the vertical interval varies, as with a nonstandard video signal. C14521 sets the time constant of this amplitude regulating servo circuit. If the total capacitance were too small, vertical linearity would be affected. In extreme cases, field-to-field vertical jitter might be seen.

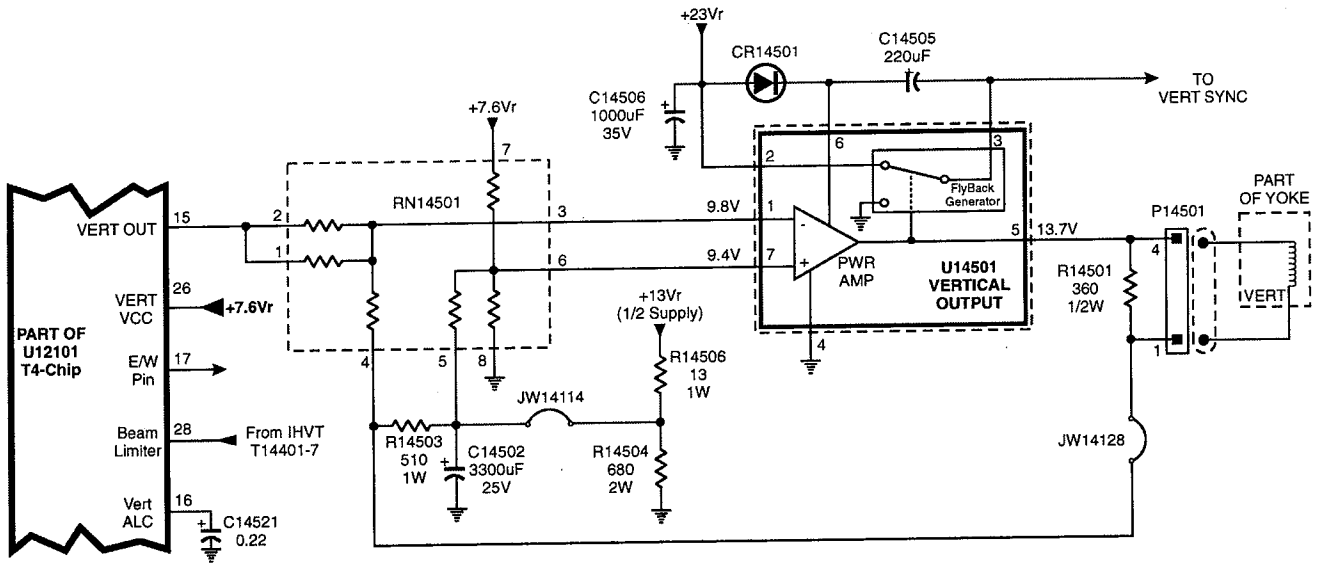


Figure 3-21, Vertical Output (Repeated)

E/W Pincushion

An E/W pincushion correction signal is generated internally by the T4-Chip and output to the pincushion correction amplifiers. It is used to correct pincushion errors in the horizontal raster. Figure 3-22 shows a typical pinchushion output waveform from U12101-17.

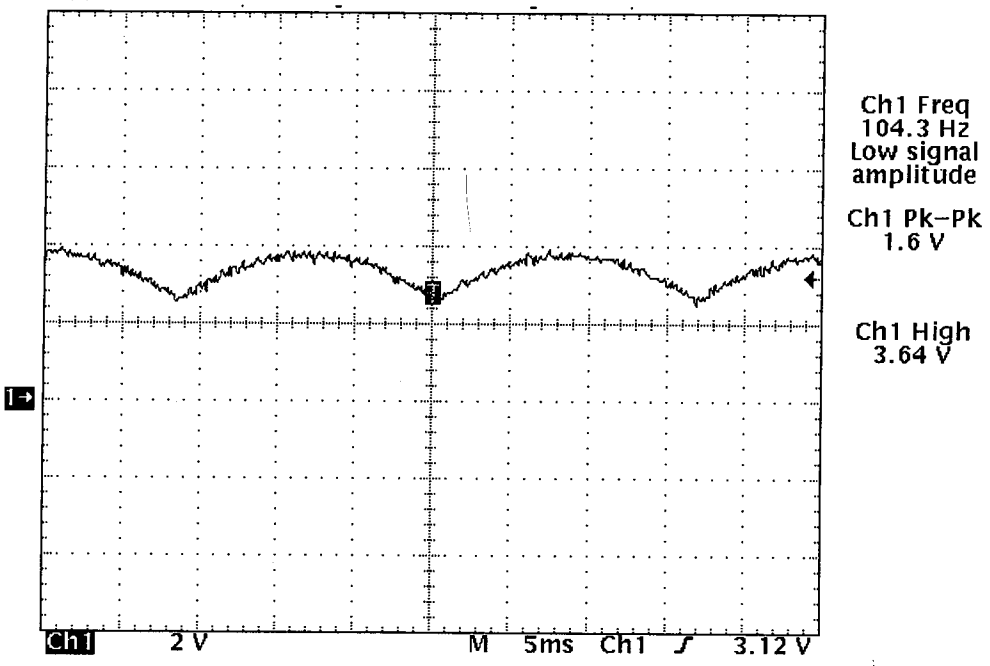


Figure 3-22, Pincushion Waveform

Troubleshooting

The vertical circuit is DC coupled and does not rely on capacitors for S-shaping and feedback. As a result, vertical troubleshooting can be accomplished with a digital volt meter and an oscilloscope.

Warning: Do not try to check the DC operation of U14501 by grounding pin 1 or applying 23 volts. Damage to U14501 or any of the direct coupled stages may result.

No Vertical Deflection

1. Check for the presence of the 23 volt supply on U14501-6 and U14501-2. If it is not present, troubleshoot the +23Vr supply. If OK, proceed to the next step.
2. Check for the half supply of approximately 13 volts at U14501-5. If it is not there, check for an open R14501. If OK, proceed to the next step.
3. Check for a 2 Vp-p vertical parabola on U14501-1. If it is not there, check U12101-15 for a 2Vp-p vertical ramp signal. If the ramp signal is present, suspect a defective U14501. If not present, proceed to the next step.
4. Check for 7.6 volts on U12101-26. If it is not there, troubleshoot the main power supply. If the voltage is correct, check U12101-16 for approximately 3.5 volts. If the voltage is wrong suspect a defective C14521.

System Control

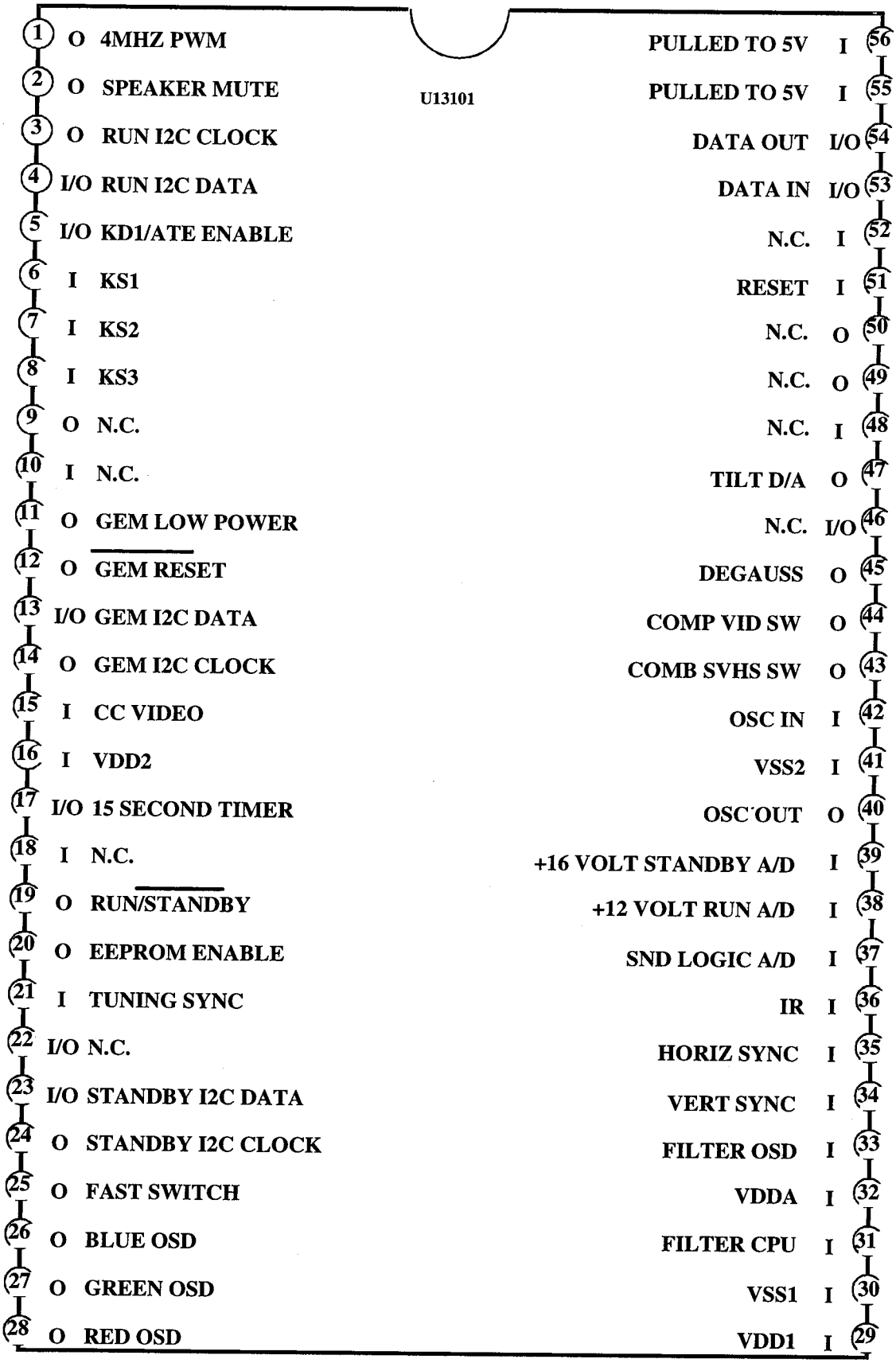
Overview

The CTC203 control system consists of a main microprocessor and a main EEPROM. The CTC203 System Control is based on a SGS-Thomson ST9 microprocessor core, the ST9296. This is the same microprocessor used in the CTC-197. It has the following features:

- 56 pin SDIP package, which includes 31 bi-directional I/O pins, eight of which are open-drain.
- On Screen Display
- Closed captioning data slicer.
- 2k RAM
- 62k ROM
- 8 channels of PWM D/A converters
- Pulse Accumulator
- Asynchronous Serial Port

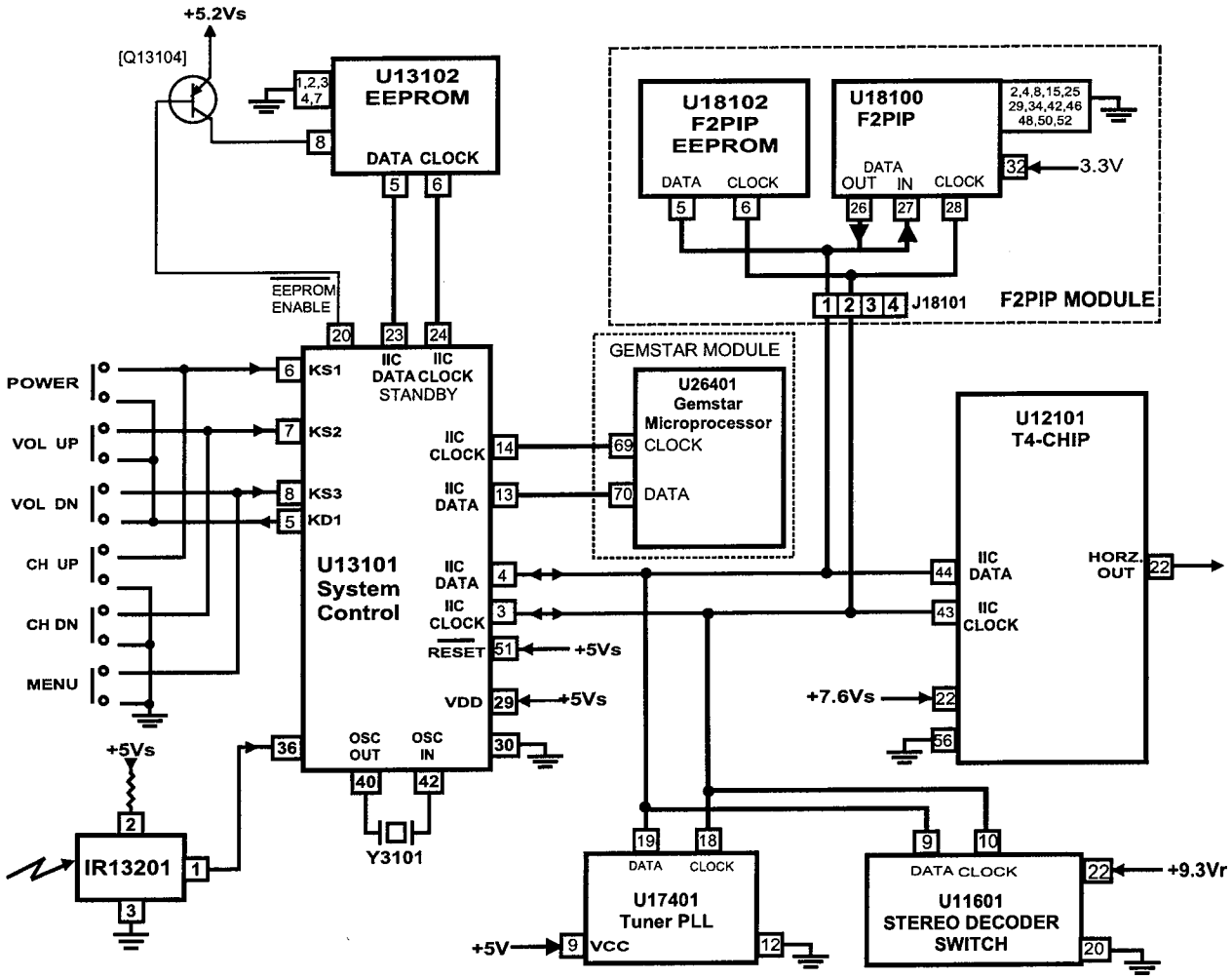
Figure 4-1 is a pinout of the microprocessor. Each pin is marked with a function and whether it is an input(I), output(O) or both (I/O)

The CTC203 chassis is a digitally controlled television receiver. System control governs the entire operation of the television. The control circuits are not only responsible for turning the set on and off, but also for aligning the different circuits such as deflection and signal. Adjustments that were aligned with a potentiometer on other chassis are now aligned digitally via the microprocessor with the values stored in the EEPROM (**E**lectrically **E**rasable **P**rogrammable **R**ead **O**nly **M**emory). This means that values can be changed by writing new values to the specific parameter. The EEPROM will hold all values written to it during and after loss of power. The EEPROM also stores certain user settings. This ensures that these settings will not be lost during long power outages.



Microprocessor Top Level Block Diagram

Figure 4-1



CTC203 SYSTEM CONTROL BLOCK DIAGRAM

Figure 4-2, System Control Block Diagram

There are three two wire IIC busses in the CTC203 chassis, called Standby, Run, and Gemstar. The Standby bus is connected to the main EEPROM, U13102. The Gemstar bus is connected to the Gemstar module only. The run bus is connected to the remainder of the IIC devices in the chassis, U17401 Tuner IC, U12101 T4-Chip, U11601 Stereo Decoder Switch and the F2PIP Module if present. The standby bus is always active, while the run bus is only active after power up. The Gemstar bus can be activated by software without powering up the remainder of the chassis. This is to allow updates to the TV Guide Plus+ material at any time via downloads from the source station.

The two wires that comprise the IIC bus are the serial data line (SDA) and the serial clock line (SCL). In each data transaction the initiating device is considered the bus master and the responding device is considered the bus slave. The bus master initiates communications by generating a START condition, a High to Low transition on the SDA line with the SCL line held high. Following this start condition, the bus master issues a device address on the SDA line (MSB first) while clocking the SCL line. The LSB of the device address is a data direction bit (R/W). The master has indicated that it will WRITE data to the slave if this bit is Low. If the bit is high, it has indicated that it will READ information from the slave. In either case the addressed slave device will respond with an acknowledge bit by pulling the SDA line Low, thereby completing the communications handshake. The corresponding data transaction, READ or WRITE, then takes place after which the master issues a STOP condition to terminate the communications session. The STOP condition is indicated by a Low to high transition on the SDA line while the SCL line is held high. The figure below is a graphical representation of the communications sequence just described. Note that all information on the bus, both device address and data, is formatted into 8 bit bytes with an acknowledge bit following each byte.

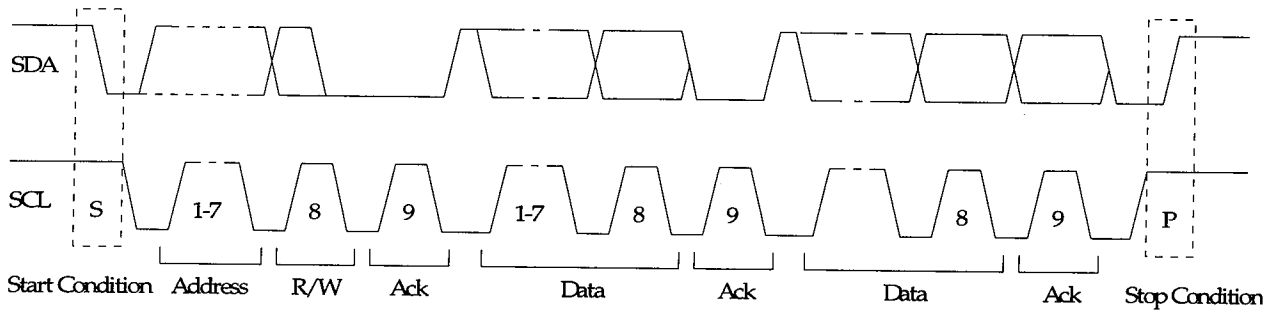


Figure 4-3, IIC Bus

Standby Supplies

Standby, when used in this application, means that the supply is always on as long as the AC cord is plugged in. These supplies are available at all times. This contrasts with the Run supplies, which only supply power when turned on by the micro.

Reset

When AC power is first applied, the reset circuit goes High after the +16Vs supply rises above approximately +11.35V. When the reset circuit goes High the microprocessor starts at the beginning of its program. There is an internal delay of about 16ms that allows the crystal oscillator time to come up and stabilize before allowing the microprocessor to run. If the standby supplies begin to go down, the reset circuit turns ON and holds U13101-51 Low. The microprocessor disconnects the busses internally and proceeds into a backup routine. The reset circuit holds U13101-51 Low during AC Power Up, brown outs and power dropouts.

Reset Timing

The following is an approximate timing diagram of the reset cycle.

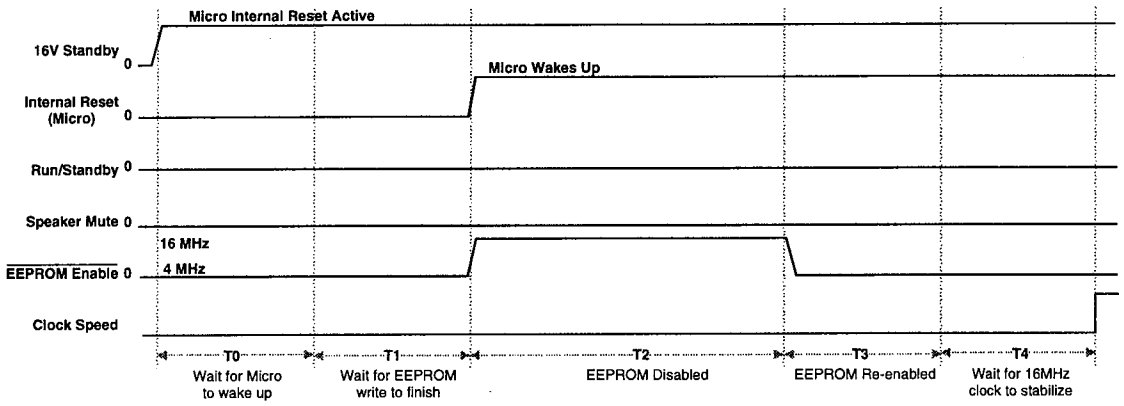


Figure 4-4, Reset Timing Diagram

Time	Wait/Action Description	Min	Typical
T0	Internal Microprocessor Reset time		1 6 msec
	Init Stacks, Mode Register, and Ports		
T1	Wait for any EEPROM writes to finish Set EEPROM Enable High to disable	10	14.7 msec
T2	Wait for EEPROM supply to decay Set EEPROM Enable Low to enable	10	12 msec
T3	Wait for EEPROM supply to stabilize Setup the 16 MHz internal clock	1	2 msec
T4	Wait for internal clock to stabilize Enable the 16 MHz clock Init the IR and Display Driver Read "batten down" data from EEPROM Initialize software modules Start 20 msec timer for power supply checks		12 msec

Reset Operation

When AC is first applied to the set the +5Vs and +16Vs begin to increase. The +5Vs to the collector of Q13501 will rise faster than the +16Vs. When the collector voltage increases to 0.7V above the base, Q13501 will turn ON. With current flowing through Q13501, bias is provided to the base of Q13503 allowing it to conduct. With Q13503 biased ON the transistor pulls the reset pin (51) Low. The reset pin will remain Low until the +16Vs rises above approximately +11.4V.

Under normal operating conditions, the voltage on the base of Q13501 is approximately +6V which reverse biases the Q13501-B keeping it from conducting. Without current flowing in Q13501, Q13503-B is pulled Low through R13511. If the +16Vs supply drops lower than +7.5V the base voltage falls to approximately +4.3V forward biasing Q13501 which begins to conduct. When Q13501 turns ON, the current flowing into the base of Q13503 will also turn it ON and pull the +5V reset line to ground initiating a reset to System Control, U13101. When Q13503 is conducting R13505 is effectively in parallel with R13504. When the +16Vs supply begins to rise it must reach approximately +11.4V before Q13501-B is high enough to reverse bias the junction. This provides about 4V of hysterisis to the circuit

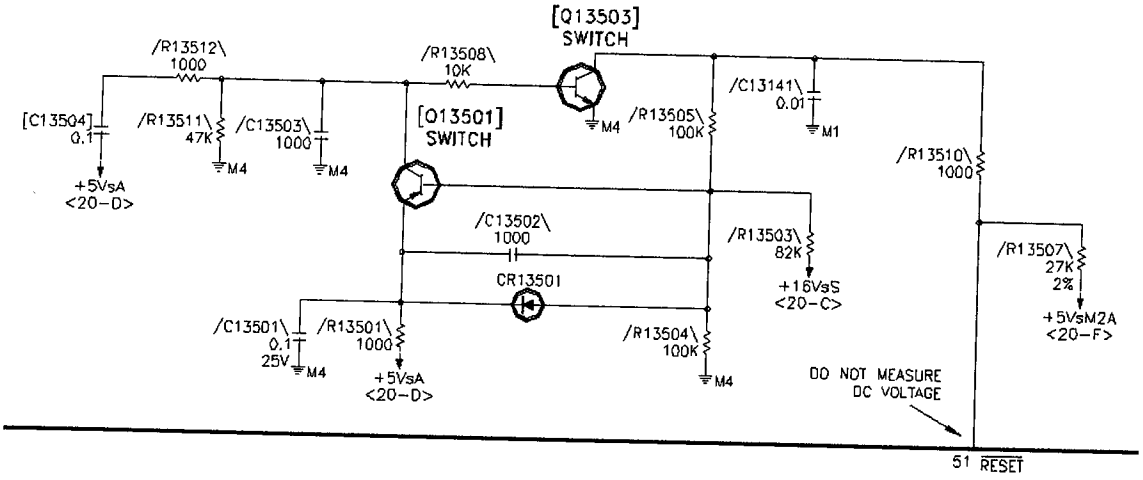


Figure 4-5, U13101 Reset Circuit

Software Detection

The +16V Standby supply is sampled directly by the microprocessor, U13101-39 via a 6-bit A/D microprocessor and is used to verify that the supply is active and within regulation, approximately 80% of its nominal voltage. Failure to meet the level specification will result in a power cycle of the entire instrument using the "batten down the hatches" routine, but **will not save the appropriate error code in the EEPROM**, since this condition is usually the result of pulling the AC plug.

The +12V Run supply is an input to U13101-38 of the microprocessor and is sampled by a 6-bit A/D used to verify the supply is active and within regulation, approximately 70% of its nominal voltage. Failure to meet the level specification will result in a power cycle of the entire instrument using the "batten down the hatches" routine **saving the appropriate error code in the EEPROM**.

The +16Vs supply and the +12Vr supply are monitored by the microprocessor using A/D's to determine if a reset condition is imminent, or brownout conditions are present. If the supplies drop the microprocessor will turn off the run supplies and activate the "batten-down-the hatches" routine and save off the following chassis operational conditions;

1) Current time
2) Current channel
3) On/Off state
4) Mute
5) Volume Setting

15 Second Timer

Once a shutdown condition occurs, a 15 second timer begins its countdown. The circuit components are connected to System Control at U13101-17. It assures that the time-of-day is maintained until the timer input on pin 17 fails to maintain a logic 1 condition. As indicated by the pin title, this normally happens about 15 seconds after a power failure. It enables the chassis to maintain the time-of-day through minor power outages or brownouts that may dip below the minimum AC supply tolerance for less than 15 seconds.

POR (Power Off Reset)

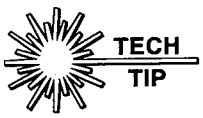
Circuitry in the T4-Chip detects when the standby-power voltage has dropped too low and shuts off deflection, effectively shutting down the set. The output of the POR detector is latched and may be read as a status bit over the serial bus by the microcomputer. If the detector is latched when the TV is ON, it is sent an OFF command followed by an ON command in order to again start the instrument. If the standby voltage is still too low when the ON command is received, the IC will stay in the OFF mode, and the process will be repeated.

User Settings

During shutdown, user settings for volume, channel, user mute, time, and on/off status will be stored in EEPROM. Most settings now are written to the EEPROM as they are changed, with no shadowing of the EEPROM in RAM. It is no longer necessary to guarantee RAM retention with this system configuration. The microprocessor has approximately 10ms to allow any writes to the EEPROM in order to store the present condition of the TV.

EEPROM Enable

When the power cord is first connected to the AC line, standby supplies come up, Q13503 resets the microprocessor by sending a HIGH to pin 51. The microprocessor controls the power to the EEPROM (U13102) through pin 20 and Q13104. During reset pin 20 goes High reverse biasing Q13104 removing the +5V from the EEPROM. After the microprocessor is reset, U13101-20 is set to a high-impedance state. R13128 pulls the base of Q13104 towards ground forward biasing Q13104, the 5.2V supply is connected to the EEPROM (U13102) turning it ON. The microprocessor then checks the EEPROM address for an acknowledgment. If the EEPROM is acknowledged, the microprocessor waits for the next command.



If there is no EEPROM acknowledgment, the microprocessor continues to try to contact the EEPROM. This can be seen on the oscilloscope as continuous data activity on the IIC data line.

The EEPROM enable circuitry of the microprocessor gives it the ability to turn off the power to the EEPROM in case the devices lock up. The EEPROM is turned off and then back on each time the TV comes out of reset and when the set "battens down the hatches" to insure it is ready for operation.

T4-Chip Power Control

The T4-Chip uses a +7.5Vr volt supply to pin 26 for Video and Vertical VCC. It is derived from the +12Vr supply which is controlled by the microprocessor Run/Stby line. The +7.6Vr supply to the T4-Chip is available only when the +12V run supply is turned ON. The power control circuitry of the microprocessor gives it the ability to turn off the power to the T4-Chip in the event the devices lock up. Because the microprocessor goes through a power up sequence every time the instrument is turned on, the T4-Chip is cycled off and then back on each time the TV is turned on. This resets the T4-Chip each time the TV is powered up assuring it is ready for operation.

Main Power Supply On/Off Control

With AC power already applied to the set, when the power button is pressed or a remote control ON command is received the video and audio mute lines are low. This assures no picture or sound can be processed accidentally by circuitry having some residual voltage supply remaining. During this time the Run/Standby signal at U13101-19 goes HIGH activating the +12Vr supply. The supplies ramp up during the next 50-400ms. When the +12Vr supply reaches about 90% of nominal, the microprocessor assumes the +7.5Vr supply derived from it is stable enough to activate the T4-Chip and it begins writing data to the T4-Chip. After this, there is a short amount of time for the Run supplies to completely stabilize before the Run IIC devices are initialized. This is also the time when auto-detect is looking for features on the instrument. When IC initialization begins, the microprocessor also stops vertical deflection and degausses the CRT.

The Hi-Fi and Line outputs are muted normally and held in a non-muted state. This is so that any power supply drop out will cause the line outputs to mute, reducing the risk to high-power amplifiers that may be connected to them. As circuit stability is established, the OSD and tuner are allowed to function. As soon as a channel is captured, video blanking is turned off allowing video to pass. When the high voltage supplies have reached normal operating voltages, video will appear on the CRT.

Data Acquisition On

In order for the Gemstar module to down load TV Guide Plus+ data when the set is off, the microprocessor must turn on several portions of the instrument. The tuner and video sections of the T4-Chip are the main components. When the instrument is in data acquisition ON, deflection is off. With no deflection, the associated power supplies derived from deflection are also off rendering the set unable to display video on the CRT. Degaussing is also disabled.

Power Down

With the set ON, if the power button is pressed or a remote control OFF command is received, the microprocessor immediately blanks video. The volume level is reduced, the speakers are muted and the T4-Chip is ordered to stop deflection. High voltage and deflection begin shutting down. The microprocessor takes the Run/Standby (U13101-19) Low, shutting down the 12Vr supply, shutting down the instrument.

Batten Down the Hatches

The "Batten Down the Hatches" sequence is one of the most important actions performed by the microprocessor. It is invoked during any problem sensed by the microprocessor and acts to save off all settings and alignments, plus an error code to cue the technician as to the possible cause of the failure. The most important function is to shut down the set as normally as possible during loss of incoming AC, whether long term or short term. The batten sequence will occur when the +16Vs supply being monitored by system control on U13101-39 drops to about +9.5V during a power up cycle, or to about 2 volts below the reading of the standby D/A from the microprocessor, U13101-39 during normal operation. The microprocessor tests the +16Vs supply starting 1.5 seconds after power up and 1.5 seconds after power down. Some power supply dip or surge is expected during start up and shut down, so 1.5 seconds was chosen to make certain any ringing or dipping of the supply had stabilized before taking a reading. This reduces the chances of an accidental batten sequence, when in reality what might be occurring is a normal power supply dip or surge during start-up or shut down.

The "Power Fatal" trigger is the +16Vs supply monitor on pin 39 of the microprocessor, U13101. Anytime after the 1.5 second power on cycle, if the +16Vs supply falls below approximately +9.5 volts the batten sequence begins. The first actions are to jettison all devices that place a high drain on the remaining residual power supply. The speaker outputs, run supplies, OSD display, Gemstar module and any other circuit not necessary to saving information to the main EEPROM are cut loose. The EEPROM is kept enabled during the next 10 milliseconds for it to complete any normal instrument data writes. After that, the EEPROM is disabled by U13101-20 of the microprocessor going HI. It is then cycled back ON. The OFF/ON cycling makes certain the EEPROM is reset and ready to accept data. When the EEPROM supply has stabilized, one more write containing the batten down the hatches device status is written.

When this sequence is completed, the microprocessor monitors the condition of the standby supply. The 15 second timer on U13101-17 tells the microprocessor how long the power has been disconnected. When the supplies return to nominal, if it has been less than 15 seconds, the set is powered up with no loss of data, including clock time. If it has been greater than 15 seconds, clock time and some other consumer set conditions are lost..

Feature Auto Detection

As with the CTC179/189, certain features of the CTC203 chassis family are auto detected. The microprocessor checks for appropriate hardware and if detected, supports that feature. If not, it assumes the feature is not supported in the chassis version and runs without it. In these instances, the set will not shutdown, but will run minus the feature. Current auto-detected features include:

- TV Guide Plus+
- F2PIP
- Number Of Jacks (0J, 3J, 5J)
- Comb Filter (none, analog, or digital (F2PIP)).
- Presence of S-Video Jack with comb filter. If F2PIP is present, S-Video selection is automatic. S-Video selection is done via menu choice for analog comb.
- Picture tilt circuit (Z-Coil). In addition to detecting the presence of the circuit on the chassis there is a bit to disable the Picture Tilt menu choice even if the circuit is present. This is to allow the Z-Coil to be left off when not required.

Run Supply Detector

As previously discussed, system control monitors the +12Vr supply directly from U13101-38 once the set has been turned on. If for any reason the run supply is not present when the set is initially turned on, the microprocessor will abort the power on sequence and try to restart the set. If after three tries the run supply is not detected, the microprocessor places the TV in the off mode. This is known as the "three strikes and you're out" sequence. Pressing the power button will restart the detection process. Remember there are only three error code locations and that every start attempt will fill one of the locations. If the set is restarted, the new error codes will only overwrite the last (third) location recorded during the previous power up attempt. The first two locations will remain the same until they are erased manually from the front panel or reset by Chipper Check. The +16Vr supply is also directly monitored by the microprocessor, U13101-39. After the 1.5 second delay at start up for the supply sag to recover, system control begins real time monitoring of the supply. If at any time the operating voltage drops farther than 2 volts, the microprocessor will enter the batten sequence.

A loss of horizontal deflection may cause the run supply detector to trip. Without the load of the horizontal deflection circuitry, Reg B+ begins a rapid climb. The power supply error amplifier, monitoring Reg B+ line for regulation, quickly shortens the duty cycle of the power supply in an attempt to reduce Reg B+. However, the +12Vr supply is still fully loaded and consequently may slump to less than the required voltage the microprocessor is looking for, causing the run detector to trip. This will cause the microprocessor to log a run supply error code, when deflection is the real problem.

Microprocessor Input Signals

Certain video and deflection signals are input to the microprocessor, U13101. The luma signal from the selected video out is buffered by Q13101 and applied to U13101-15, the closed caption decoder. Video out of the T4-Chip, U12101-42 is buffered by Q13103 and applied to U13101-21 for channel tuning (see tuning algorithms for more information). Vertical and horizontal deflection pulses are applied to U13101 pins 34 and 35 respectively to provide a synchronization reference for correct positioning of the On Screen Display.

Microprocessor Pin Assignments

Understanding the role of the microprocessor in the operation of the instrument will greatly assist the technician in any troubleshooting. Many of the outputs and inputs of the microprocessor are digital, which means they are either a logic 0 or 1. They can be measured with a standard DVM as either a HIGH (2.5–5.0 volts) or a LOW (<2.5 volts). Activity on data and clocks can be observed and compared to Figures 4-6 and 4-7.

On an oscilloscope very little data line detail can be distinguished, but the presence of activity is generally all that is required to confirm operation. If the data line is flat, it first must be understood what communication should be taking place before assuming that no activity means a defect. Accessing a feature, such as PIP or input switching should cause activity on the data line.

If the clock line is flat, there is probably microprocessor trouble. With either line, if trouble is suspected always begin by "ohming" the line to check for shorts.

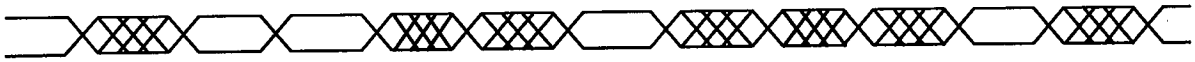


Figure 4-6, Data Line Activity

Figure 4-7, Clock Line Activity

1	O	4MHZ PWM	PULLED TO 5V	I	56
2	O	SPEAKER MUTE	PULLED TO 5V	I	55
3	O	RUN I2C CLOCK	DATA OUT	I/O	54
4	I/O	RUN I2C DATA	DATA IN	I/O	53
5	I/O	KD1/ATE ENABLE	N.C.	I	52
6	I	KS1	RESET	I	51
7	I	KS2	N.C.	O	50
8	I	KS3	N.C.	O	49
9	O	N.C.	N.C.	I	48
10	I	N.C.	TILT D/A	O	47
11	O	GEM LOW POWER	N.C.	I/O	46
12	O	$\overline{\text{GEM RESET}}$	DEGAUSS	O	45
13	I/O	GEM I2C DATA	COMP VID SW	O	44
14	O	GEM I2C CLOCK	COMB SVHS SW	O	43
15	I	CC VIDEO	OSC IN	I	42
16	I	VDD2	VSS2	I	41
17	I/O	15 SECOND TIMER	OSC OUT	O	40
18	I	N.C.	+16 VOLT STANDBY A/D	I	39
19	O	$\overline{\text{RUN/STANDBY}}$	+12 VOLT RUN A/D	I	38
20	O	EEPROM ENABLE	SND LOGIC A/D	I	37
21	I	TUNING SYNC	IR	I	36
22	I/O	N.C.	HORIZ SYNC	I	35
23	I/O	STANDBY I2C DATA	VERT SYNC	I	34
24	O	STANDBY I2C CLOCK	FILTER OSD	I	33
25	O	FAST SWITCH	VDDA	I	32
26	O	BLUE OSD	FILTER CPU	I	31
27	O	GREEN OSD	VSS1	I	30
28	O	RED OSD	VDD1	I	29

U13101

Microprocessor Top Level Block Diagram

Figure 4-8, U13101 Microprocessor Pinout

U13101 Pin Functions

Following is a description of the main system control microprocessor functions. The pin number is first and then the function is outlined briefly. Last is a description of the port type; Input, Output or Input/Output. Many ports are used during manufacturing by ATE (Automated Test Equipment).

1. 4MHZ_PWM: This is a 4MHz output used for testing the microprocessor oscillator. Used by ATE in the factory. **Output**
2. SPEAKER_MUTE: The SPEAKER_MUTE output is used to mute the left/right audio to the power amps. **Output**
3. Run IIC CLOCK: The Run IIC CLK line is an output line which conforms to the Philips IIC Bus Specification. The maximum clock rate is 100kHz. The Run IIC CLK line is operational only when the receiver is in "Run" mode (Run mode is defined as either the TV is on or data acquisition for TV Guide+ timed download is active). **Output**
4. Run IIC DATA: The Run IIC Data line is an I/O line, which conforms to the Philips IIC Bus Specification. The Run IIC CLK line is operational only when the receiver is in "Run" mode (Run mode is defined as either the TV is on or data acquisition for TV Guide+ timed download is active). **I/O**
5. KD1/ATE ENABLE: The KD1 line is configured as an output that switches between logic 0 and 1 levels to detect key presses from the front panel assembly. **Output**
6. KS1: The KS1 line is one of three lines (KS1, KS2, KS3) configured as inputs to detect front panel key presses. The lines are normally high (5V) and are pulled to ground by a key closure. **Input**
7. KS2: The KS2 line is one of three lines (KS1, KS2, KS3) configured as inputs to detect key presses. The lines are normally high (5V) and are pulled to ground by a key closure. **Input**
8. KS3: The KS3 line is one of three lines (KS1, KS2, KS3) configured as inputs to detect key presses. The lines are normally high (5V) and are pulled to ground by a key closure **Input**
9. N.C.
10. N.C.
11. GEM_LOW POWER: The TV Guide Plus+ Low Power Mode input is used to tell the TV Guide Plus+ microprocessor that the +5V supply used by the TV Guide Plus+ microprocessor will drop out within 50 msec. The TV Guide Plus+ microprocessor will then properly power down. **Input**
12. GEM RESET: The GM_RESET resets the GemStar Module. The reset is activated to give the Gemstar module advanced warning to perform its power down sequence, once "batten down the hatches" has been initiated. **Output**

13. GEM_ IIC DATA: The GEM IIC DATA line is an I/O line, which conforms to the Philips IIC Bus Specification. The maximum clock rate is 100kHz. The GEM IIC Data line is operational as long as the receiver is plugged in. **I/O**

14. GEM_ IIC _CLK: The GEM IIC CLK line is an output line, which conforms to the Philips IIC Bus Specification. The maximum clock rate is 100kHz. The GEM_IIC_CLK line is operational as long as the receiver is plugged in. **Output**

15. CC Video: CC Video is an input to the control system. The line contains 1.0Vp-p (negative going sync) NTSC video. This is used to provide the Closed Caption signal to the microprocessor for decoding into usable text. Video input level 1.0Vp-p +/-.2V (from 100 IRE to -40 IRE sync tip) DC Level:2.5V nominal **Input**

16. VDD2: The microcomputer and EEPROM use the +5V_STBY1. Input Level 5.0V +/-8% **VDD**

17. 15 Second Timer: The 15 second timer determines whether time-of-day clock information is discarded after a power dropout. If a dropout lasts longer than 15 seconds, the time-of-day information will be cleared. If it is less than 15 seconds, it will be retained. **Input**

18. N.C.

19. RUN/STANDBY: The RUN/STBY is a buffered output line used to turn on the Run supplies. Run mode is selected when the output is a logic 1. Logic 1>3.5V, Logic 0 <.6V **Output**

20. EEPROM ENABLE: The EEPROM ENABLE output is used to control the standby supplies going to the EEPROM. This line allows the EEPROM to be reset in the event of an SCR latch. **Output**

21. TUNING_SYNC: The TUNING_SYNC input is composite video (negative going sync) from the demodulated IF output of the T4-Chip, which is separated by a control system sync separator. The separated sync is sampled by the microprocessor to determine the presence of valid video during channel tuning. Input Video 1.0Vp-p(from 100 IRE to -40 IRE sync tip) **Input**

22. **N.C.**

23. STANDBY IIC DATA: The STBY IIC Data line is an I/O line, which conforms to the Philips IIC Bus Specification. The maximum clock rate is 100kHz. The standby IIC Data line is operational as long as the receiver is plugged in. **I/O**

24. STANDBY IIC CLOCK: The STBY IIC CLK line is an output line, which conforms to the Philips IIC Bus Specification. The maximum clock rate is 100kHz. The standby IIC CLK line is operational as long as the receiver is plugged in. **Output**

25. Fast Switch (FSW): The fast switch line is the output of a 1-bit D/A. The output is active high when OSD is present. Logic 1; >2.7V (OSD active), Logic 0; <0.4V (OSD not active) **Output**

26. Blue OSD: The blue on-screen display signal is the output of a 3-bit D/A. The pin voltage is 1.0Vp-p (100IRE) and is divided down to 0.5Vp-p for roughly (70IRE) OSD characters. Rise and fall times after the filter are nominally 70nsec. Output level 0.5Vp-p (for nominal 70 IRE OSD) **Output**

27. Green OSD: The green on-screen display signal is the output of a 3-bit D/A. The pin voltage is 1.0Vp-p (100IRE) and is divided down to 0.5Vp-p for roughly (70IRE) OSD characters. Rise and fall times after the filter are nominally 70nsec. Output level 0.5Vp-p (for nominal 70 IRE OSD) **Output**

28. Red OSD: The red on-screen display signal is the output of a 3-bit D/A. The pin voltage is 1.0Vp-p (100IRE) and is divided down to 0.5Vp-p for roughly (70IRE) OSD characters. Rise and fall times after the filter are nominally 70nsec. Output level 0.5Vp-p (for nominal 70 IRE OSD) **Output**

29. VDD1: +5V Standby Supply Voltage. Input Level +5V +/- 8% **VDD1**

30. VSS1: Ground return path **Ground**

31. Filter CPU: Filter used to keep various unwanted signals from interfering with microprocessor functions **Input**

32. VDDA: +5V Standby Supply Voltage. **Input Level +5V +/- 8% VDDA**

33. Filter OSD: Filter used to keep various unwanted signals from interfering with microprocessor functions, in this case with OSD. **Input**

34. VERTICAL SYNC: The Vertical Sync input signal to the control system is used to synchronize the OSD signal to vertical. Only the leading edge is used. The Vertical Sync signal is used to blank the OSD during vertical retrace. An internal delay is used in the main microprocessor to insure that the leading edges of Vertical and Horizontal do not overlap. A single value of the internal Vertical delay is intended for all chassis. A spike filter, which ignores any glitch of < 2usec after an active edge is detected was added to prevent double vertical pulses on PTV instruments. Input Level 0-5.2V max DC (active high) Logic 1 >3.5V (Vertical active); Logic 0 <1.0V (Vertical not active) **Input**

35. Horiz Sync or "FBP": The FBP (FlyBack Pulse) input signal to the control system is used to synchronize the microprocessor OSD to the flyback pulse. Only the leading edge is used. The width of the Horizontal Sync signal derived from the Flyback Pulse is used to blank OSD during horizontal retrace. The 5V level of the flyback waveform was chosen to minimize OSD variation with flyback loading. **Input**

36. IR: IR is the infrared input to the microcomputer accepting IR from the Remote Control IR Receiver. The circuitry allows for a simultaneous 2nd IR receiver on a separate FPA for use on consoles in addition to an IR input from the Smart Plug interface which is used on commercial products. **Input**

37. SND_LOGIC_A/D: The SND_LOGIC_A/D is sampled by the 6 bit A/D in the microprocessor and used to control a compression algorithm that adjusts the volume control in the T4-Chip. The SND_LOGIC_A/D comes from a fullwave detector of the audio signal after the AUX switch so that both the "off_air" and AUX audio levels can be compressed. Input Level 0 - 5V **Input**

38. +12V RUN A/D: The +12V RUN supply input is sampled by a 6-bit A/D in the microprocessor and used to verify that the supply is active and within regulation. Failure to meet the level specification will result in a power cycle of the entire instrument using the "batten down the hatches" routine which will save off the appropriate error code is the EEPROM. Input Level +12V ±20% (for valid 12V_RUN) **Input**

39. +16V STANDBY A/D: The +16V supply is input to the +16VSTBY_A/D pin of the microprocessor and sampled by a 6-bit A/D in the microprocessor used to verify that the supply is active and within regulation. The actual voltage into the +16VSTBY_A/D pin is 32% of the +16Vs supply. +16Vs is polled every 20msec, and transients less than 2msec should be ignored due to deglitching in the software. Failure to meet the level specification will result in a power cycle of the entire instrument using the "batten down the hatches" routine, but will not save the appropriate error code in the EEPROM since this condition is usually the result of pulling the AC plug. **Input**

40. OSC OUT: 4 MHz clock crystal **Output**

41. VSS2: Ground return path **Ground**

42. OSC IN: 4 MHz clock crystal **Input**

43. COMB_SVID_SW: (for enhanced CTC203) Video switch control line used to switch between the internal COMB filter output or an external SVHS source. On start-up, this pin is used as an input to detect which module is being used. **Output**

44. COMP_VID_SW: Video switch control line used to switch between internal tuner video and an external composite video source. On start-up, this pin is used as an input to detect which module is being used. **Output**

45. DEGAUSS: The Degauss signal is a buffered output signal sent to operate the degauss relay. Once a power-on sequence has been initiated and the power supplies reach a specified voltage, the Degauss line is held low (Degauss active) for approximately 1.5 seconds. Under normal conditions the Degauss line is high. The Degauss buffer transistor is located in the Deflection area. **Output**

46. N.C.

47. TILT D/A: The Tilt_D/A output allows the user to compensate for the affects of the earth's magnetic field on the raster alignment. The Tilt D/A will allow a minimum of 64 customer adjustment points. **Output**

48. N.C.

49. N.C.

50. N.C.

51. RESET: Input to the Control System providing a reference voltage for sensing the level of the +16Vs Supply. Normally 5.2 volts. **Input**

52. N.C.

53. DATA_IN: UART input line to the micro. It will be used by the MCR module to communicate to the main micro. MCR is for commercial product. **Input**

54. DATA_OUT: The Data Out line is the output from a UART in the micro. It will be used by the MCR to communicate to the main micro. **Output**

55. Pulled to 5Vs through 100K. **Input**

56. Pulled to 5Vs through 100K. **Input**

IR Input

Infrared remote signals are amplified by IR13201 and appear at U13101 pin 36 as 5Vp-p negative going data pulses. When no IR is received, the DC level at U13101-36 is 5V. IR3401 is powered by the +5Vs supply. There is no power indicator LED on the normal CTC203 chassis.

OSD Circuit

The CTC203 ***O***n ***S***creen ***D***isplay circuit consists of red, green and blue analog signals from U13101 pins 28, 27 and 26 respectively. These signals along with the FSW (fast switch) signal from U13101-25 are sent to the T4-Chip U16201 pins 33, 34, 35 and 36. These on screen display signals include user menus and also any closed caption information. The FSW signal is also used by the T4-Chip to turn off incoming video during the time interval OSD is active, preventing incoming video from appearing in the OSD.

Closed Captioning

In this discussion Closed Captioning is meant to include Captioning for the hearing impaired, Text Mode data and Extended Data Services (EDS) that may also be broadcast. Closed Captioning data may be transmitted on Line 21 during the Vertical Blanking Interval (VBI). Data may be transmitted using either field 1 or 2 in an NTSC video signal. The closed captioning information is read by the microprocessor on U13101-15.

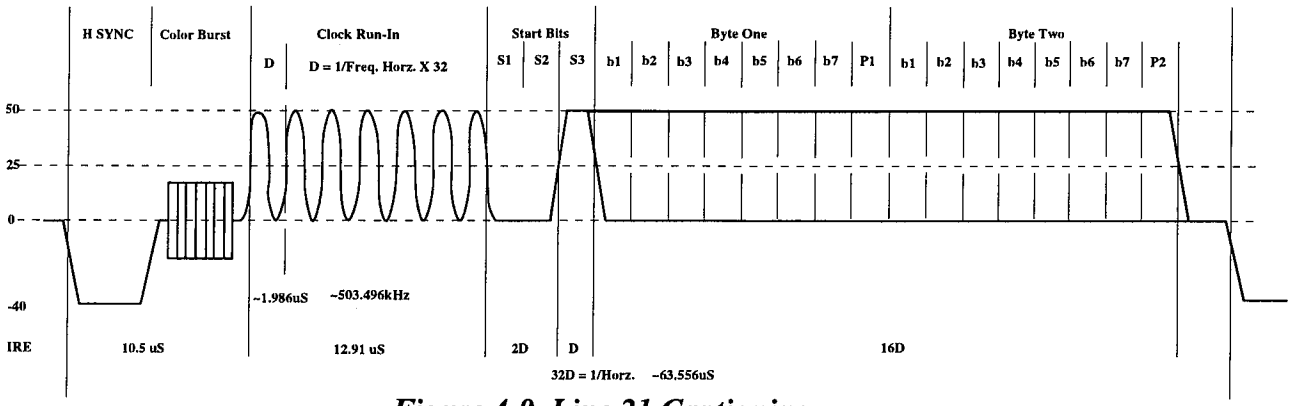


Figure 4-9, Line 21 Captioning

Figure 4-9 is a representation of the horizontal scan line 21 in an NTSC video signal. Captioning data (D) is defined as having a period that is one thirty-second of the horizontal scan rate. If the scan rate is approximately 15734.26Hz then D = 1/15734.26 X 32 , D =~503.4965kHz or a period of ~1.986uS. The transmission consists of a Run-in clock, 3 start bits and 2 bytes of data. A byte of data is made up of 7 bits plus one parity bit. The midpoint of the clock (half amplitude or 25 IRE) should be the same as the midpoint for the start bits and data bits.

Captioning data is detected using a data slicer internal to the microprocessor. The data slicer accepts the incoming composite video as an AC coupled signal through a 1μF capacitor to the CC video pin. Captioning data is synchronized to the microprocessor by a sequence of 6.5 clock cycles (run-in clock) of 503KHz after the horizontal sync and color burst that is in phase and with the same amplitude as the data. A zero-zero-one bit start sequence and 2 bytes of data, with each byte including an odd parity bit, follows the run-in clock.

The data slicer is able to extract Closed Caption (CC) data from a composite video signal broadcast in agreement with the EIA-608 format. The slicing level for data is controlled automatically by hardware. When used in conjunction with the OSD, the data slicer allows for Captioning data to be displayed.

The black level of the CCVIDEO signal is clamped internally to a reference voltage of approximately 2.0V. The clamped video signal is then applied to a sync slicer for sync extraction by comparing it with a sync slicing level voltage Vref set at -13 IRE.

The CCVIDEO signal is also applied to another voltage comparator called the data slicer for the data extraction. The slicing level Vslice, for normal signals, 25 IRE, is automatically generated by hardware. The output signal is forced high when the input signal exceeds Vslice indicating the presence of a bit of data. The output is fed into the data processor where it is processed for the selected line of OSD.

V-Chip

The "V-Chip" is integrated into the CTC203 circuitry via the System Control Microprocessor U13101. Using the Closed Captioning input it receives and processes a data stream sent by a broadcaster or other program provider that contains program content advisory data. When programmed by the viewer, the instrument can respond to the advisory data by blocking content that the viewer finds objectionable. Closed Captioning circuitry is used to incorporate program content advisory along with additional software functionality that was required in the receiver as well as encoded program ratings in the TV signal.

Instruments can receive 525 lines of information split into two equal fields. Field 1 of line 21 of the vertical blanking interval (VBI) is reserved for closed captioning information. Field 2 may carry captioning as well as program information such as content advisories. A voluntary industry standard has been established for encoding and transmitting such information on line 21, field 2.

The Parental Controls menu allows users to program the instrument such that others cannot view certain programs, channels, or use the front panel controls

XRP (X-Ray Protection)

Circuitry in the T4-Chip detects possibly unsafe conditions in the instrument and shuts down automatically. The output of the XRP-detector is latched and may be read as a status bit over the IIC bus by the microcomputer. This XRP latch is reset by setting the ON/OFF control bit in the T-Chip to OFF, and therefore may be read only when the instrument is on.

When an XRP fault is reported to the control microcomputer (The XRP detection componentry is fully described in the deflection section), it turns the main run supply and horizontal output off, waits for 1.5 seconds, and then turns the instrument back on. If the XRP fault is not cleared, the microprocessor will cycle the set OFF/ON 3 times (*Three Strikes, You're Out*) before shutting OFF completely.

Periodic Update

All bus registers are updated every 6 seconds under normal conditions. All user settings will be stored in EEPROM during the update. They are also written to the EEPROM as they are changed, with no shadowing of the EEPROM in RAM. It is no longer necessary to guarantee RAM retention with this system configuration.

IIC Bus

When the set is first plugged in, the Standby IIC data and clock lines (U13101 pins 23 & 24) will have about 50 milliseconds of 5Vp-p data and clock. The pulses occur at approximately 50 kHz. After the initial data and clock activity are sent by the microprocessor, both the standby data and clock lines normally go low and remain.

Before sending out an IIC command, software checks that lines are high. If something is clamping the bus, software will remove power from the EEPROM for 30 milliseconds then attempt to send the command again. If the bus is working, the microprocessor will write an error code (bus latch) to the service menu location.

When an attempt is made to turn the set on, the RUN/STANDBY line (U13101-19) will be set high and the T4-Chip will be toggled off. Then an ON command will be sent. The microprocessor will check Run Data and Clock lines the same as it did the Standby lines before attempting to send the command. If the set does not turn on, check the level of the of the Run Data and Clock lines at the time the RUN/STANDBY pin goes high. The data line should have information within 40 milliseconds after the RUN/STANDBY line goes high. If both do not go high, something is loading one of the lines. The microprocessor should have written the appropriate error code in the service menu location.

Three Strikes and You're Out

The "Three Strikes and You're Out" routine is active for power supply drops and XRP faults. The routine was designed to prevent re-occurring faults from further damaging the instrument. Normally, the microprocessor sends out commands, then waits for an acknowledgment the command was received. Software attempts to re-send any commands when it does not receive the acknowledgment. If the command is not acknowledged after a third attempt to send it, (the *third* non-acknowledgement) the "batten down the hatches" sequence is initiated. "Batten" stores off information to the EEPROM and then removes power from the instrument. Software will then attempt to restore power to the instrument. If 3-4 faults are detected within one minute, the instrument will remain in the off state, awaiting the customer to turn it back on. If less than 3 faults occur within a minute, the instrument will turn off for 2-3 seconds and then automatically turn back on.

Service Menu

The CTC203 chassis has a limited built-in service menu to facilitate instrument alignments.

All other alignments must be performed with a computer using Chipper Check™, TCE's computer-based troubleshooting/alignment software.

To enter the on-board service menu, turn the set ON, press and hold the **Menu** button. Then while continuing to hold the **Menu** button, press and release the **Power** button. Then press and release the **Volume+** button. The instrument should immediately display a one line menu on the screen similar to Figure 4-10.

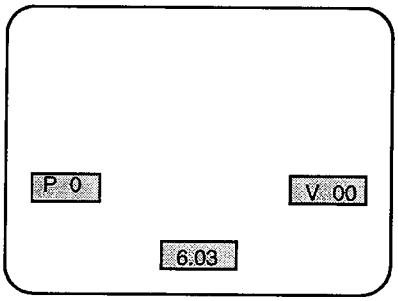


Figure 4-10, Service Menu Screen

The decimal value on the left is the parameter number and the decimal value on the right is the current value of that parameter. The **Channel-Up** and **Channel-Down** buttons increment and decrement the parameter number, while the **Volume+** and **Volume-** buttons adjust the current value of that parameter. When parameters are modified, the corresponding T4-Chip registers and EEPROM locations are updated. The **Power-On**, **Power-Off** buttons on the menu, or **Power-Toggle** button on the front panel exit service mode. The number below and in the center is the software version number.

Under normal conditions, failure of an IIC device to acknowledge a query will prevent the TV from turning on. Because a possible reason for needing service is a failed bus IC, the normal check for acknowledge is disabled in the service mode. If an IIC device has failed, its address will be stored in the error code area.

When the service mode is first turned on, the parameter will be 0. This 0 parameter is used for security purposes to protect the factory alignments from inadvertent modification by requiring a specific value be selected before other parameters may be accessed. If channel up is pressed while in parameter 0, the service mode will be exited. A security parameter must be selected before the service technician proceeds. To select the security parameter, while in parameter 0, change the value (using volume up/down) to 76. **Note**: The value will wrap around (0 - 254..255..0..1...)

Parameters

There are a limited set of instrument parameters available to the technician from the front panel of the set. All other alignments or adjustments are accessible via Chipper Check™ troubleshooting software and a PC.

P:	Parameter Name	Value Range	Notes and Comments
00	Security Parameter	76	Cannot advance to parameters until value is met
01	Error Detection (1st)	???	First Error Code
02	Error Detection (2nd)	???	Second Error Code
03	Error Detection (last)	???	Third Error Code
04	Horiz. Phase	00 .. 15	
05	EW DC (Width)	00 .. 31	
06	EW Amplitude	00 .. 15	
07	EW Tilt	00 .. 15	
08	Top Corner Correction	00 .. 07	
09	Bottom Corner Correction	00 .. 07	
10	Vertical D.C.	00 .. 63	
11	Vertical Size	00 .. 127	
12	Vertical Countdown Mode	00 .. 03	0 = Standard; 1 = Non-Standard; 2 = 50 Hz; 3 = 48 Hz
13	Red Bias	00 .. 127	See "Service Line"
14	Green Bias	00 .. 127	See "Service Line"
15	Blue Bias	00 .. 127	See "Service Line"
16	Red Drive	00 .. 63	
17	Green Drive	00 .. 63	
18	Blue Drive	00 .. 63	
19	Gemstar H OSD Position	00 .. 255	For Gemstar only
20	Gemstar V OSD Position	00 .. 255	For Gemstar only
21	Gemstar H PIP Position	00 .. 255	For Gemstar only
22	Gemstar V PIP Position	00 .. 255	For Gemstar only
23	Gemstar PIP Window Vertical Size	00 .. 13	For Gemstar only

Service Line

When the R, G, or B Bias Parameters (13,14, or 15) are selected, the **Menu** button will be used to toggle a setup line with the following characteristics (performed in the order given):

- Video - Is blanked by setting the IF_AGC_Defeat bit high in the T4-Chip.
- Black Level - Load the T4-Chip Brightness Register (14) with data from EEPROM.
- Vertical is Killed.
- Sub-Brightness is loaded into the T4-Chip from the EEPROM.

When the setup line is toggled off via the **Menu** button the following occurs:

- Video - Is unblanked by setting the IF_AGC_Defeat bit low in the T4Chip.
- Black Level - is set to the User Value
- Vertical is unKilled.

If the R, G, or B Bias Parameters (13, 14, and 15) is changed and the service mode is exited via the **Power-Off**, or **Power-Toggle** buttons the screen will turn green

Troubleshooting

The system control circuit controls every function of the TV. A failure in this circuit can cause the entire TV to malfunction. Provided U13101, U13102, and U16201 are functioning, the set can be forced to turn on in the service mode by holding down the MENU button and pressing POWER and VOLUME UP in that order. Entering the service menu and reading the error codes will lead the technician to the defective circuit area. In some cases, the set will not be able to be forced on even in the service mode. In these cases, the set will most likely try to start three times and then stop or remain silent and do nothing at all. When the technician encounters this, the TCE troubleshooting and alignment software, Chipper Check™, may be used to read the EEPROM error codes to begin repair efforts.

Error Codes

Upon certain errors occurring in the chassis, an error code will be stored in the EEPROM. This error code is displayed to the service technician as the value located at parameter 01, 02 and 03. If a 0 is stored in the value, there have been no errors. If there is a nonzero value, however, the following table describes what error occurred. If multiple errors occur, the first error is stored in 01, the second error is stored in 02 and **the last error to occur is stored in 03**. Because only the last error location (03) is incremented upon each additional error, the error codes should all be reset to 0 upon completion of the service effort so that a three error code history will be available in the future. The error code numbers are changed just like the other alignment parameters

Error code:		Chassis:	Error:
HEX	**DEC**	**POWER CONTROL ERRORS**	
00	0	ALL	No Errors
01	1	ALL	16V_STBY fault
03	3	ALL	12V_RUN fault
08	8	ALL	T4-Chip XRP (X-ray protection)
09	9	ALL	T4-Chip POR (power on reset)
0A	10	w/F2PIP	F2PIP POR
0B	11	ALL	Stereo Decoder POR
10	16	ALL	Run IIC bus latched
12	18	ALL	Standby IIC bus latched
HEX	**DEC**	**IIC ACKNOWLEDGE ERRORS**	
22	34	w/Gemstar	Gemstar bus fault
2C	44	w/ F2PIP	F2PIP fault
80	128	ALL	Stereo Decoder fault
BA	186	ALL	T4chip fault
C4	196	ALL	Main Tuner PLL bus fault
C6	198	ALL	Main Tuner DAC bus fault

If an IC error code is found that is the same as one in the table, then that device did not acknowledge. For example, if the error code is 128, the Stereo Decoder (U11601) did not acknowledge. If the error code is the same as any in the table, but incremented by 1 (129) then the read register did not respond. The problem

indicated is still the Stereo Decoder. Other error codes may indicate a failure condition some other place in the chassis, such as the power supply. It is important to understand how these error codes are detected by the system control circuitry so they can be interpreted correctly and used accordingly. Most of the error codes are self-explanatory.

There are two power supply error codes; 1 and 3. They monitor the run and standby supplies for any voltages dipping below a preset level. An explanation of the microprocessors role in monitoring the power supplies and incoming AC power has been given in previous discussions. Unfortunately, failures 1 and 3 above will prevent the television from turning on, making the error codes impossible to read via the service menu. These error codes can only be checked by reading the EEPROM directly. This can be accomplished by using computer based alignment software called "Chipper Check™." Chipper Check™ allows the service technician to perform digital alignments, read the diagnostic error codes and check the hardware integrity of EEPROM. This can literally reduce repair time by hours by accelerating the alignment process, preventing unnecessary parts orders and by giving the technician a means of checking the EEPROM even when the TV will not turn on. Chipper Check™ is now available. Contact TCE Publications at (502) 491-8110 for more information.

No Remote Control

Check for an idle voltage of +5V (logic HI) at U13101-36, or at JW13107. Press any IR button and check for a series of 5Vp-p pulses. If the pulses are not present, suspect a defective IR13201 or a missing +5V standby supply to IR13201

NOTE: Some IR receivers may be oversensitive to high energy compact fluorescent lighting. If pin 36 shows 5Vp-p of constant noise, remove the lighting and recheck. Also note that the keyboard input has priority over the IR input. If a keyboard button is stuck, the IR input will be ignored.

No Keyboard Operation

The keyboard drive line, U13101-5, should have a 5Vp-p square wave on it at all times. The sense lines, pins 6, 7 and 8 should be at logic HIGH(5V). Power, Volume-up and Volume-down buttons will cause the respective sense lines to follow the drive line. Menu, Channel-up and Channel-down will cause the sense lines to go low (ground).

No OSD

While trying to display OSD, trace the red, green and blue OSD signals from U13101 pins 28, 27 and 26 to U16201 pins 34, 35 and 36 respectively. Also check for the presence of horizontal and vertical sync at U13101 pins 34 and 35.

No Closed Caption Display

In the CTC203, the same circuitry that drives the closed caption circuitry also drives OSD. If there is OSD but no closed caption, check the video signal at U13101-15. If there is no OSD, troubleshoot the OSD circuitry.

XRP Shutdown

An XRP code (#8) in the service menu signifies that an error condition exists that may cause the set to emit X-Rays. The set will exhibit the *"Three Strikes and You're Out"* routine . The XRP trip code is sent back to the microprocessor from the T4-Chip. The XRP circuitry must be examined. XRP is covered in the deflection section.

POR (Power On Reset)

Several of the IIC devices have internal POR (***P***ower ***O***n ***R***eset) registers that indicate when the power supply voltage has dropped below where the internal registers can guarantee reliable data transfers. The microprocessor reads this data as part of its Periodic Update routine. If a supply has dropped below the set levels in any of the IC's, the set will be turned off and then go into the *"Three Strikes and You're Out"* routine. If the set does not start back up, read the error codes with Chipper Check™ to determine which IC has generated the POR.

Run Bus Latch

This will occur when either the RUN Data or Clock lines are clamped to ground. This could be caused by a circuit path short in the Data or Clock lines or the power supply to the IIC device shorting to ground or pulled high. The error codes will indicate which device to troubleshoot.

NOTE: ***Any IC connected to the IIC Bus must be fully powered to prevent protection diodes, used to prevent ESD on the bus line, from clamping the bus.***

Power Supply Error

The microprocessor monitors two supplies, the +12Vr and the +16Vs directly and one, the +7.5Vs indirectly. If the error codes indicate a supply error, refer to the Power Supply section on troubleshooting.

Dead Set - Degauss Relay Clicks

If the television tries to start three times and then stops (you can hear the clicking sound of the Degauss relay energizing), this means the Microprocessor (U13101) and EEPROM (U13102) are communicating. When the power button is pressed check for a HIGH signal from the RUN/STANDBY pin 19, U13101. If it is present the control circuit is OK and the problem is most likely power supply and/or deflection related. Use Chipper Check™ to read the EEPROM error codes. See the Error Code listing to determine the cause of the problem and to begin repair efforts. You can also perform the following checks.

1. Check the +16Vs supply input at either pin 39 U13101 or JW14134 near T14101 for proper voltage. If not present refer to the Power Supply troubleshooting section.

2. When the power button is pressed, the RUN/STANDBY line at U13101-19 goes HIGH. This turns the +12 Volt Run supply ON. Check U14104-3 (regulator), or U13101-38, (micro) for +12 Volts. If not present refer to Power Supply troubleshooting section.

3. Check the power supply operation to the T4-Chip by checking the input U12101-26. This is the +7.6 Volt supply voltage which is produced when the +12 Volt Run supply is switched ON. If not present check the +7.6 Volt regulator, U14150.

4. When the power button is pressed check pins 3 and 4, U13101, the Run IIC clock and data lines. If the data or clock lines do not go to +5 volts, unsolder any devices attached to the bus and see if the pads goes up to +5V. If they do, suspect a defective device. If they do not go up, check the +5V standby supply to pull-ups R13166 and R13169.

Dead Set - No Clicking Relay

1. Check the +5.2 Volt standby supply at U13101-29. If not present go to Power Supply troubleshooting section.

2. Press the power button and check for U13101-19 to go HIGH(+5V). If it does, go to Power Supply troubleshooting section. If it does not, go to the next step.

3. Check U13101-51 reset, for +5V. If not present check the microprocessor reset circuit, Q13501 and Q13503, for proper operation. If present continue to the next step.

4. Check U13102-8 EEPROM, for +5V standby supply. If not present check for a LOW on U13101-20. If low and +5V is present at the emitter of Q13104 the transistor is defective. If present continue to next step

5. Check U13101 pins 40 and 42 for ~4.5Vp-p 4MHz sine-wave (using X10 probe). If it is not present, suspect a defective Y13101, C13106, C13107, R13107 or U13101. If the oscillator is present, go to the next step.

6. Check the Keyboard sense lines, pins 6, 7 and 8, U13101. The sense lines should be +5 Volts with no buttons pressed. Press and hold the power button, pin 6, KS1 should be pulled LOW. If not check the continuity to the switches. If it goes LOW check pin 5, KD1 (Keyboard Drive1) for a 5 Volt 40msec square wave. If present continue to next step.

7. Monitor U13101 pins 23 and 24 with an oscilloscope set at 10 msec/div. When 120 V.A.C. is applied to the set, check for the presence of momentary data and clock pulses after the data line rises to 5 volts. If the data and clock lines goes HIGH and the pulses appear, suspect a defective U13102 (EEPROM).

8. If the data or clock lines does not go to +5 volts, unsolder pins 23 and 24 of U13101 and see if the pads goes up to +5V. If they do not go up, check the +5V pull-up supply from R13142 and R13139. If present unsolder pins 5 and 6 of U13102 and see if the pads goes up to +5V. If they do, U13102 is most likely loading down the bus and is defective.

If the data line goes HIGH but the negative going pulses do not appear, unsolder the clock line (U13101- pin 24) and check for continuous pulses from pin 23. If the pulses do not appear, suspect a problem with U13101. If the transmission is continuous check the power supplies again or suspect a defective U13102 (EEPROM).

Tuner

Tuner Basics

A television tuner receives (or selectively *tunes*) a 6MHz bandwidth RF (Radio Frequency) carrier that contains audio and video information and converts it to a common IF signal (Intermediate Frequency). The IF signal is demodulated by the television into its audio and video components. All tuners work on the principle of a tuned circuit whose resonant frequency determines what channel is tuned. By changing the tuned circuits' resonant frequency, different RF carriers (channels) are selected. Before discussing the different sections that comprise the tuner's circuitry, it is appropriate to review certain fundamental concepts of inductors, capacitors and varactors. These components play a major role in all tuned circuits.

Inductors

Remember, an inductor is simply a coil of wire. The ability of a coil to oppose a change in current is a measure of the inductance *L* of the coil. Inductance is measured in henries (H) although most inductors will be in micro henries (uH) 10^{-6} H. For inductors in series, the total inductance is found in the same manner as resistors in series, figure 5. Likewise, the total inductance of inductors in parallel is found in the same manner as resistors in parallel, Figure 5-1. The main idea to remember here is inductors added in *parallel reduce* the total inductance and inductors added in *series increase* the total inductance.

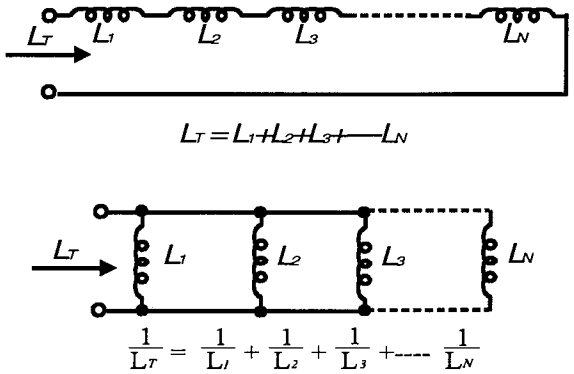


Figure 5-1, Series and Parallel Inductors

Capacitors

Capacitors are components made of two parallel conducting plates separated by an insulating material. A capacitor stores a charge on its plates. The storage capacity *C* is measured in Farads (F). The farad is generally too large a unit for most tuner applications so the pico farad (pF) 10^{-12} F is used. Total capacitance is calculated in the opposite manner as inductance, Figure 5-2. Capacitors in *parallel increase* total capacitance and capacitors in *series decrease* total capacitance.

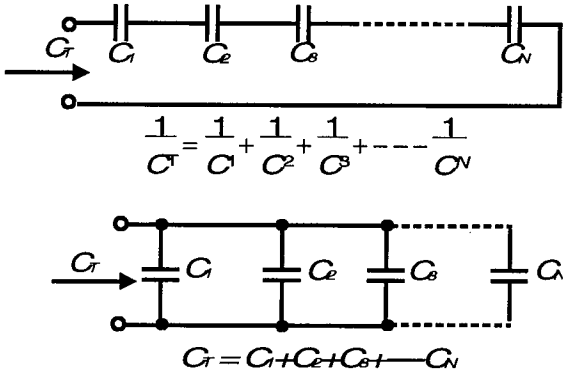


Figure 5-2, Series and Parallel Capacitors

These two fundamental concepts are essential to understanding and troubleshooting tuner circuits. The circuit in Figure 5-3 is a simple parallel resonant band-pass filter circuit, similar to what would be found in a tuner. The purpose of the band-pass filter is to allow the desired or tuned frequency to pass while attenuating other frequencies that might be present. The band-pass frequency is determined by a relationship as shown. The main point here is *decreasing the capacitance and/or inductance will raise the resonant frequency. Increasing the capacitance and/or inductance will lower the resonant frequency.*

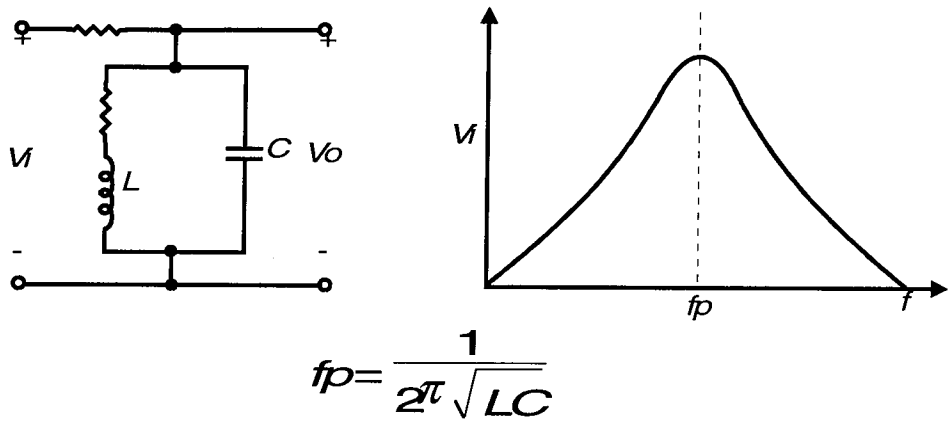


Figure 5-3, Band Pass Filter

Varactor Diode

One of the major components found in an electronic tuner is the varactor diode. The varactor acts like a voltage variable capacitor. An *increase in reverse bias* across the diode causes the *capacitance to decrease*. Conversely, a *decrease in reverse bias* causes its *capacitance to increase*. This allows the resonant frequency of a tuned circuit to be changed by applying a specific tuning voltage, Figure 5-4.

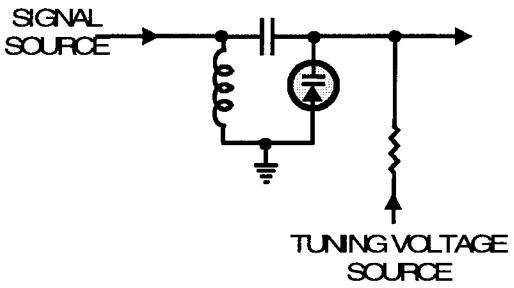


Figure 5-4, Basic Varactor Tuning Circuit

Input Filter

A tuner is composed of the basic elements shown in Figure 5-5. The front end of a tuner has a network that filters out unwanted FM and IF frequencies that may be present. It also contains a singled tuned filter that selects the frequency of the desired channel and inputs this signal to the RF amplifier.

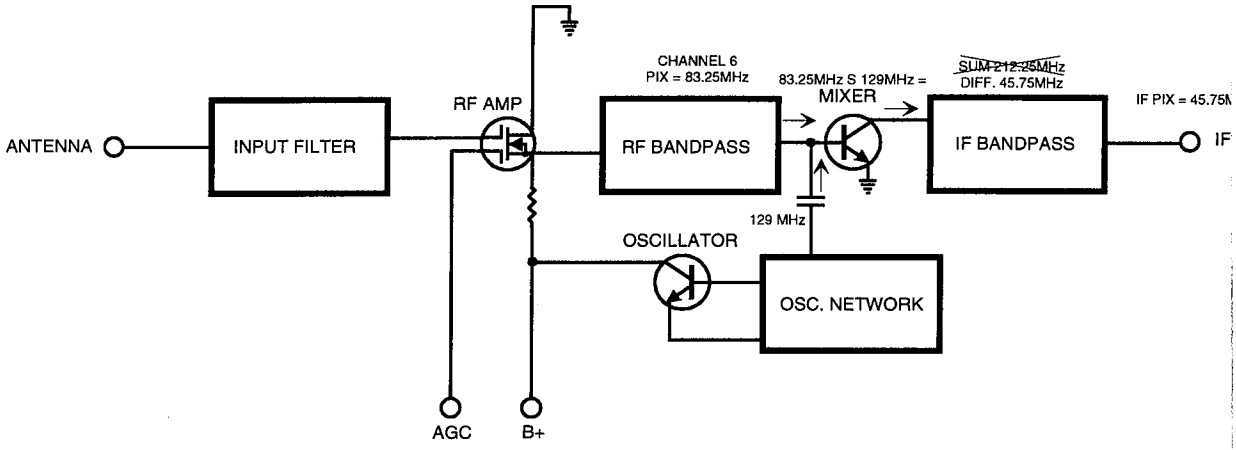


Figure 5-5, Basic Tuner

RF Amplifier

The RF amplifiers use dual gate depletion type MOS FET's (Metal Oxide Semiconductor Field Effect Transistors). These transistors are very high impedance (in the mega ohms) voltage controlled devices that function very much like vacuum tubes. The N-channel depletion type MOSFET's are normally "on" without any type of gate bias. When a negative voltage is applied to the gate with respect to the source, drain current flow is reduced or pinched off entirely if the reverse bias is sufficient. Conversely, a positive voltage on the gate with respect to the source will increase drain current flow to a point. Dual gate MOS FET's have two gates both of which affect drain current. In RF amplifier configurations, the RF signal is input on Gate 1 and the AGC (Automatic Gain Control) voltage is applied to Gate 2. As the AGC voltage rises, more drain current is produced increasing the output of the respective RF stage. As the AGC voltage decreases, the output of the RF stage decreases. These fundamental principles are important when troubleshooting.

RF Band-pass

The RF band-pass is a double-tuned filter that receives the amplified signal from the RF amplifier and re-tunes it. This performs "sharp" tuning of the RF signal to obtain greater selectivity. It also performs some impedance matching to the latter stages of the tuner.

Oscillator / Mixer / IF Band-pass

The oscillator network comprises the local oscillator with its control circuitry. The oscillator generates a signal that is beat or heterodyned against the incoming RF signal. This is done to obtain the IF picture frequency of 45.75MHz. To accomplish this, the oscillator frequency is set 45.75MHz higher than the incoming RF signal. The two signals are "beat" or heterodyned together in the mixer stage. Using channel 6 as an example, the picture frequency of 83.25 MHz is heterodyned with an oscillator frequency of 129MHz. This produces a sum signal of 212.25MHz and a difference signal of 45.75MHz. The IF band-pass extracts the difference signal which produces the channel's video carrier at 45.75 MHz, the chroma carrier at 42.17MHz and the audio carrier at 41.25MHz. For each new channel the local oscillator frequency is changed to the channel frequency + 45.75MHZ. This allows all channels to produce the same IF frequencies.

PLL / Frequency Synthesizer

The local oscillator frequency must change over a wide range to convert the many channels to the IF frequency. The local oscillator in modern electronic tuners, and more importantly the tuner in the CTC203 chassis, uses a frequency synthesizer to control the oscillator. A frequency synthesizer is made up of a PLL (Phase Lock Loop) and a programmable divider circuit.

A basic PLL block diagram is shown in Figure 5-6. A voltage controlled oscillator (VCO) sends a frequency sample back to a comparator. The comparator compares the sample frequency of the oscillator to a reference signal derived from a crystal controlled oscillator. When the oscillator is off frequency, the comparator generates an error voltage that corrects the oscillator. The VCO will stay locked to the reference oscillator.

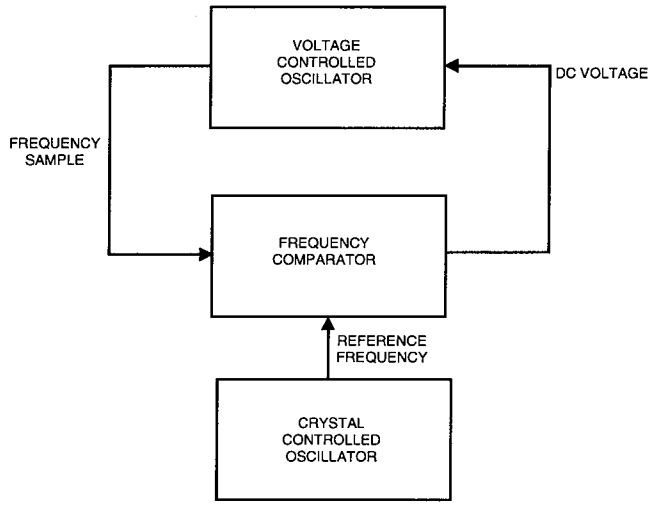


Figure 5-6, Basic Phase Locked Loop (PLL)

Adding a programmable divider to the PLL enables the oscillator to be locked at different frequencies. Division logic, usually supplied by a microprocessor, sets a divide ratio in the frequency divider. The divided down frequency is compared against the reference frequency. The comparator generates a correction voltage to keep the oscillator locked to the desired frequency, Figure 5-7. By changing the frequency divider, the PLL is able to "synthesize" different frequencies.

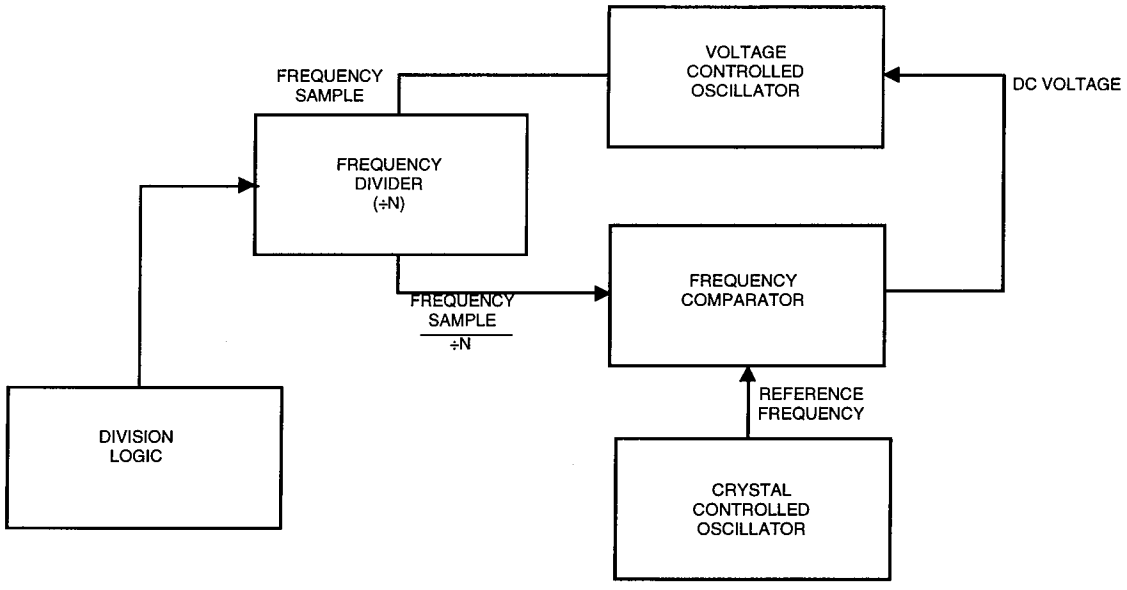


Figure 5-7, Frequency Synthesizer

CTC203 Tuner

Overview

Two tuner versions are available for the CTC203 chassis. Both TOB (Tuner On-Board) and a discrete tuner module are used, depending upon the chassis version. The module tuner will be described later. The standard tuner is very similar to the CTC185 tuner. It utilizes TOB (Tuner On-board) topography surrounded by a zinc alloy tuner wrap. The primary differences include:

- Eliminated the Isolation Box (Hot/Cold Barrier)
- Modified tuner wrap/covers

Because the tuner on-board is part of the main chassis, the tuner must be repaired to the component level rather than replacing the tuner as a complete assembly. Although repairing the tuner may be new for some, it is no different than working on other discrete sections of the TV. A basic knowledge of tuner theory, a good voltmeter and TCE Chipper Check™ troubleshooting and alignment software will enable the technician to repair most tuner on-board malfunctions.

Operation

The CTC203 tuner divides the frequency spectrum into three frequency bands. Remember, especially in the low band, channel numbers are not necessarilly in order. Frequencies are progressive.

Band 1 (Low VHF Channels 02 - 17)

Band 2 (Upper VHF Channels 18 - 50)

Band 3 (UHF Channels 51 - 125)

The tuner is controlled by the main microprocessor U13101. The micro is attached to U17401(PS/PLL/DAC) in the tuner by the Run I^2C bus. When a channel is selected by the user the micro sends information to U17401 in order to tune the desired channel. The information includes which band to select, the LO frequency to synthesize, the tuning value for the single tuned filter and the primary and secondary tuning values for the double tuned filters. Alignment values for 18 channels are stored in the main EEPROM, U13102. If a channel is selected other than one of the alignment channels then the microprocessor does a linear interpolation to determine the values and sends those values to U17401.

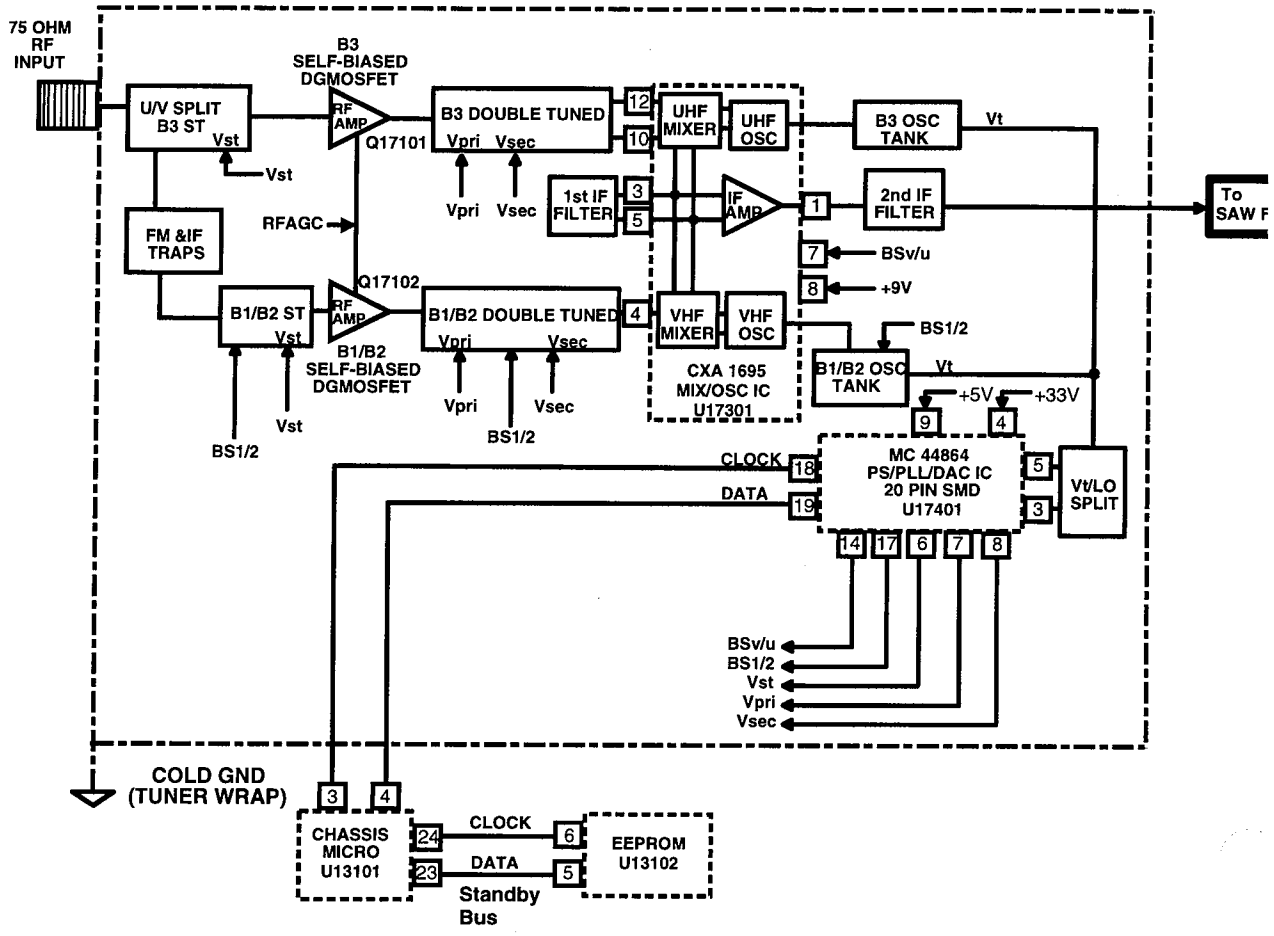


Figure 5-8, CTC203 Tuner Block Diagram

Figure 5-8 shows a block diagram for the CTC203 tuner. RF from the RF input, "F" connector, is applied to the UHF/VHF splitter network. The RF signal is split into UHF and VHF frequency paths and sent to their respective tuning networks. If the desired channel is UHF then the single tuned filter is aligned by Vst a voltage from a D\A (Digital to Analog Converter) in U17401. If the selected channel is VHF then the single tuned filter is tuned by a combination Vst and BS1/2 depending on which VHF band is selected.

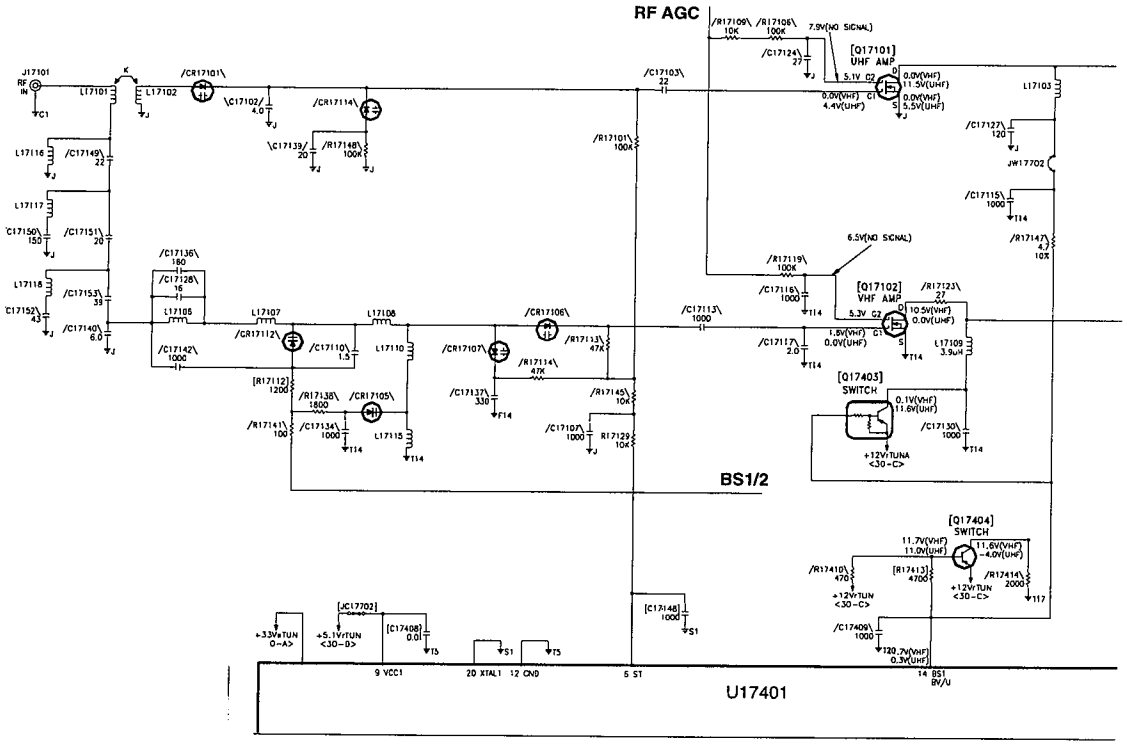


Figure 5-9, RF Amplifiers

Figure 5-9 is a simplified view of the RF input, single tuned filters and amplifier section of the tuner on the CTC203. The VHF circuitry includes portions of the single tuned filter. Voltage ST is applied to both single tuned filters (VHF/UHF) and BS1/2 is applied to the VHF single tuned filter to adjust it for whichever channel is selected. BSv/u is used to select which path, VHF or UHF is active. To select VHF the base of Q17104 is allowed to go to +12 which reverse biases the transistor. This removes +12V from the UHF RF Amp Q17101 and also from the base of Q17103. Q17103 becomes forward biased which connects the +12V to the VHF RF Amp. When BSv/u goes Low the base of Q17104 is forward biased which supplies +12V to the UHF RF Amp, Q17101, and to the base of Q17103. Q17103 becomes reversed biased removing +12V from the VHF RF Amp, Q17102.

Q17101 and Q17102 are Dual gate MOS FET's (Metal Oxide Semiconductor Field Effect Transistors) used to amplify the RF. The RF AGC voltage from the IF circuitry is input to G2 on the transistors to adjust the gain of the tuner for varied signal strengths. The amplified signal is then applied to the double tuned filter.

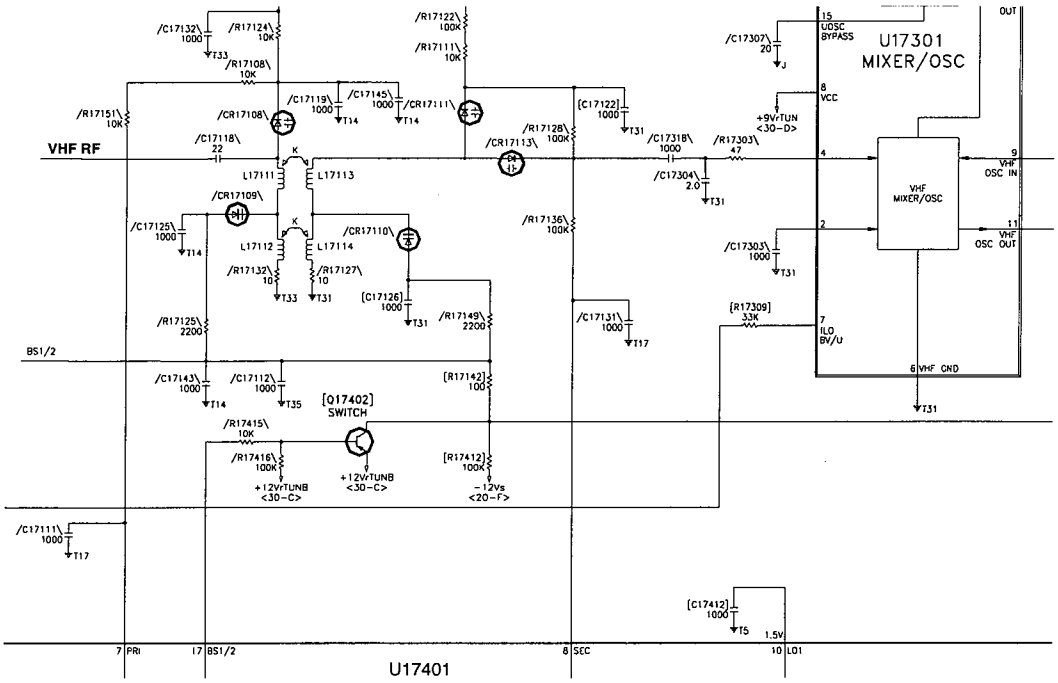


Figure 5-10, VHF Double Tuned Filter

Figure 5-10 is a simplified schematic of the VHF double tuned filter in the CTC203 tuner. Voltages PRI (pin7), SEC (pin 8) and BS1/2 (pin 17) from U17401 are applied to the filter to tune it. The filtered signal is applied to the inputs of U17301.

U17401 contains a PLL section and a DAC (Digital to Analog Converter) section and is controlled by U13101, microprocessor, through the Run I^2C bus. The PLL section contains all of the functions required to control the UHF and VHF VCOs, voltage controlled oscillators, in U17301. It generates the tuning voltage (pin 5) and additional control signals. The D to A section generates three varactor voltages, ST (pin 6), PRI (pin 7) and SEC (Pin 8), in order to feed all of the varactors of the tuner which are individually optimized control voltages for the frequency being tuned. The three D to A converters have a resolution of 6 bits (5 bits plus sign). The analog output voltages are DC. The converters are buffered to the analog outputs by operational amplifiers with an output voltage range that is equal to the tuning voltage range (about 0 to 30V). The output voltages of the D to A converters are equal to the tuning voltage plus a positive or negative offset of up to 31 steps. The op. amps. are arranged such that a positive or negative offset can be generated from the tuning voltage. During the automatic alignment one first lets the PLL lock to the appropriate frequency and then searches for the optimum of the other varactor voltages.

The UHF or VHF signal is input to the U17301 UHF or VHF mixer circuits. U17301 has a VCO for both UHF and VHF and mixers for VHF/CATV and UHF bands. BS1 U/V is input to pin 7 and is used to switch between bands. The tuning voltage is input to both the UHF and VHF VCO sections. The mixer beats the RF signal with the output of the oscillator circuit, whichever section is active. This produces the 6MHz wide IF (intermediate frequency) signal with the video signal located at 45.75 MHz. The IC also includes an IF amplifier which is output to pin 1.

Alignment values stored in the EEPROM (U13201) for 18 "alignment channels" provide the settings for the single tuned, primary and secondary filter outputs from U17401. Linear interpolation is used to adjust the voltages for these tuning networks across the entire range of channels tuned by this system. The alignment of these 18 "alignment channels" is critical. See the CTC203 service data for specific alignment instructions. The higher the tuning voltage, the more effect the alignments have on the tuning voltage. This is because it takes more voltage change at higher tuning voltages to get the same change in capacitance in the varactor diode. This is a characteristic of varactor diodes. The alignment channels and the full channel frequency allocations are shown in Appendix A at the end of this manual.

Modular Tuner

In some versions of the CTC203 chassis, a modular tuner is used. This tuner resembles previous tuner *cans* used prior to the introduction of tuner-on-board (TOB) technology. At the present time, TCE plans to implement a modular tuner in all CTC185 and CTC203 chassis beginning with the Fall, 1999 production model runs.

There are no alignments of the RF stages in the modular tuner required, however an RF AGC Delay chassis alignment will be needed if is is replaced. The slight differences between this alignment on TOB chassis and chassis using the tuner module are identified later.

The tuner is a single conversion module covering the Broadcast and CATV RF spectrum from 47MHz through 801 MHz in three bands. It requires six connections to the main chassis plus an RF input. In this case, the module has been designed to sit directly on the CTC203 chassis. The six connections are;

- RF AGC,
- IIC Data,
- IIC Clock,
- +5V,
- +33V,
- IF Output.

In addition, to avoid a change in the rear panel, an RF connector will be added to the panel with an RF cable connecting it to the module using a phono connection.

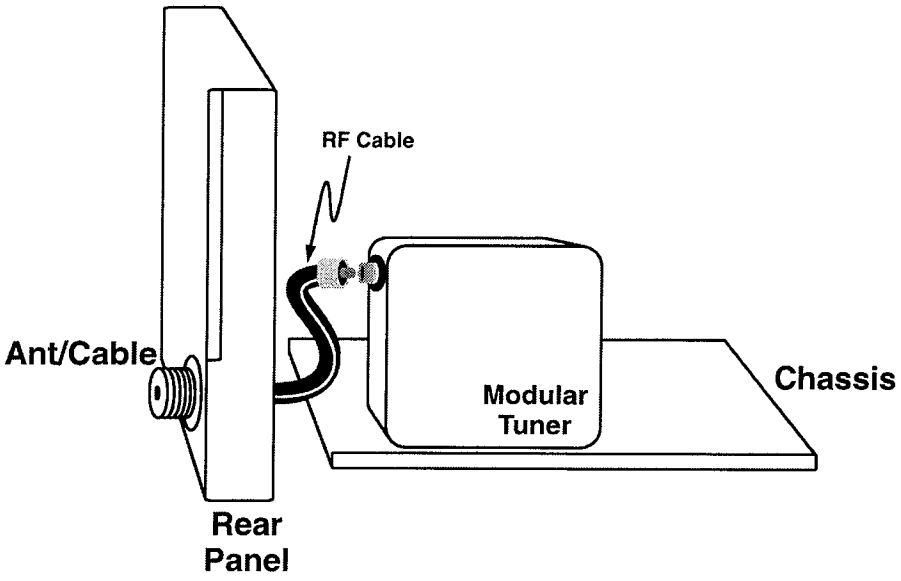


Figure 5-11, Tuner Module Location and Connection

Modular Tuner Troubleshooting

There are no field adjustments or alignments associated directly with the modular tuner. If tuning failure is suspected, follow these steps.

1. Check the IF output from the tuner module. If there is around 400mVp-p, 45.75MHz signal level, the tuner is probably OK. Move to the Video/IF sections.
2. Check the +5V and +33V supplies for proper operation. Note the normal supply tolerance of ±10% apply to the +5V supply, however the +33V tuning supply within ±5%. If not OK, troubleshoot the defective supply.
3. Probe the IIC data and clock lines using the normal troubleshooting methods associated with these signals.
4. Monitor the RF AGC line. Normal range is around +2.0V. If possible, change channels while monitoring the AGC. It should go high (>4.0V), then return to around +2.0V after the channel is captured.

Modular Tuner Replacement

If the modular tuner is replaced, it will not require any direct alignments. However instrument level adjustments, those required to "mate" the tuner with the chassis, will be needed. In the case of the modular tuner, only the RF AGC Delay adjustment is required.

RF ACG Adjustment

1. Turn the set on and allow at least a 30 second warmup period prior to beginning this adjustment.
2. Although the adjustment requires no tuner input, the technician should supply an active channel 6 signal to the antenna input and tune the set to this signal to properly initialize the tuner.
3. Apply an 45.75 MHz IF signal at 224mVp-p to the input of the SAW Filter, SF12301-1. (The TOB uses 316mVp-p for this adjustment.)
4. Set the RF AGC Delay alignment to zero using Chipper Check™ while monitoring the RF AGC line at U12101-5 with a DVM. Begin incrementing the value from zero until the RF AGC is ≥ +2.0V (±20%). (TOB uses ≥ +3.2V.) The RF AGC Delay alignment is now complete.

TOB Troubleshooting

Troubleshooting the TOB is best accomplished with a digital multimeter and TCE troubleshooting and alignment software, Chipper Check™. By making voltage and resistance checks, tuner failures can be isolated in a reasonable amount of time. Certain precautions should, however, be observed. Always put the shields back on after servicing and solder them if they were unsoldered. Make sure none of the coils in the tuner are moved or in any way repositioned (this will prevent making painstaking coil alignments later). Solder connections should be clean and smooth. Do not use more solder than is necessary.

If any of the varactor diodes are replaced in either the VHF circuits (CR17106, CR17107, CR17108, CR17111, CR17113 and CR17302 or UHF circuits (CR17101, CR17102, CR17103, CR17114, CR17301 and CR17304), all the diodes in the respective circuit must be changed. The replacement diodes are matched for capacitance characteristics and come as a set. If these guidelines are not followed, the tuner cannot be aligned correctly and will tune channels poorly. The stock numbers for the diode kits containing the matched diodes is 215492 (CR17101...) and 215494 (CR17106...).

Troubleshooting

TCE troubleshooting and alignment software, Chipper Check™, is used to read the EEPROM codes and is required to realign the turner. Note: Before aligning the tuner you should always save the current values of the EEPROM.

Instruments with GEMSTAR

Either reset or disconnect the GEMSTAR Module when troubleshooting the TUNER. When an instrument with GEMSTAR is setup to use a Cable box, the GEMSTAR module passes the commands for Channel Up/Down to the Cable box. The GEMSTAR will change the channel number OSD according to what channel is stored in the scan list. The instrument's tuner will be locked to the input channel for the Cable box. If the instrument's tuner voltages are measured they will not change even though the channel number OSD is changing.

One Band Inoperative

If the tuner will tune channels on all bands but one, limit troubleshooting to the band specific circuitry. Obviously, if one band is functional, U13101, U13102, and at least part of U17401 and U17301 are working properly.

1. Check the +5V, +12V, -12V supply voltages to the tuner.
2. If the problem is only VHF low (2- 6) or VHF hi (7 -13), make sure the BS 1/2 band switching voltage from pin 17, U17401 turns On/Off. If it does check that the band switching voltage from the collector of Q17402 turns on (or off) CR17112, CR17105, CR17109, and CR17110.
3. If the problem is that only one of VHF or UHF is present. Check to make sure the BS u/v band switching voltage from pin 14, U17401 turns On/Off. If it does check that Q17404 and Q17403 are being switched properly and that the biasing on the respective RF amplifier MOSFET(Q17101-UHF, Q17102-VHF) is correct.

Picture Present But Not Good

1. Check the AGC voltage
2. Check all the supply voltages to the tuner: +5V, +12V, -12V and +33V.
3. Check single tuned, primary and secondary tuning voltages (see voltage charts at the end of this section).
4. Check for the correct voltages on U17401.
5. Check for the correct EEPROM values by trying to improve one channel by realigning the D/A's (make sure to record the original value in order to restore it if alignment does not fix the problem).
6. Go to the "No Tuning" symptom below and check RF AGC response.

No Tuning

1. Verify channel numbers change on the screen. If the OSD does not respond to channel change commands, the problem is in another circuit. Start with the troubleshooting section in the *system control circuit.*
2. Check all the supply voltages to the tuner: +5V, +12V, -12V and +33V.
3. Check for the correct band switching voltage on pins 14, and 17 of U17401, pin 7 of U17301, and the collector of Q17402.
4. Check the tuning voltage on U17401 pin 5 and compare it to the voltage chart. Note: If the tuning voltage is stuck HI or LO, there is a problem in the PLL loop. Check for a 4MHz oscillator signal on Y17401. Depending on the loading of the oscilloscope, it should be around 1Vpp with a X10 probe
5. Check the LO voltage at the varactors CR17301, CR17304, and CR17302. The voltage should increase as channels go up in number in a band and decrease as channels come down in number. If the voltage is missing, check the path between U17401 pin 5 and varactors. Also check for a leaky or shorted CR17301, CR17302, and CR17304.
6. Check the single tuned, primary and secondary varactor diode tuning voltages.
7. Check the RF AGC response. Attenuate service modulator output. RF AGC voltage should increase.
8. Check the MOSFET bias on Q17101 and Q17102.
9. Check IF output on pin 1 of U17301.

IF Circuit

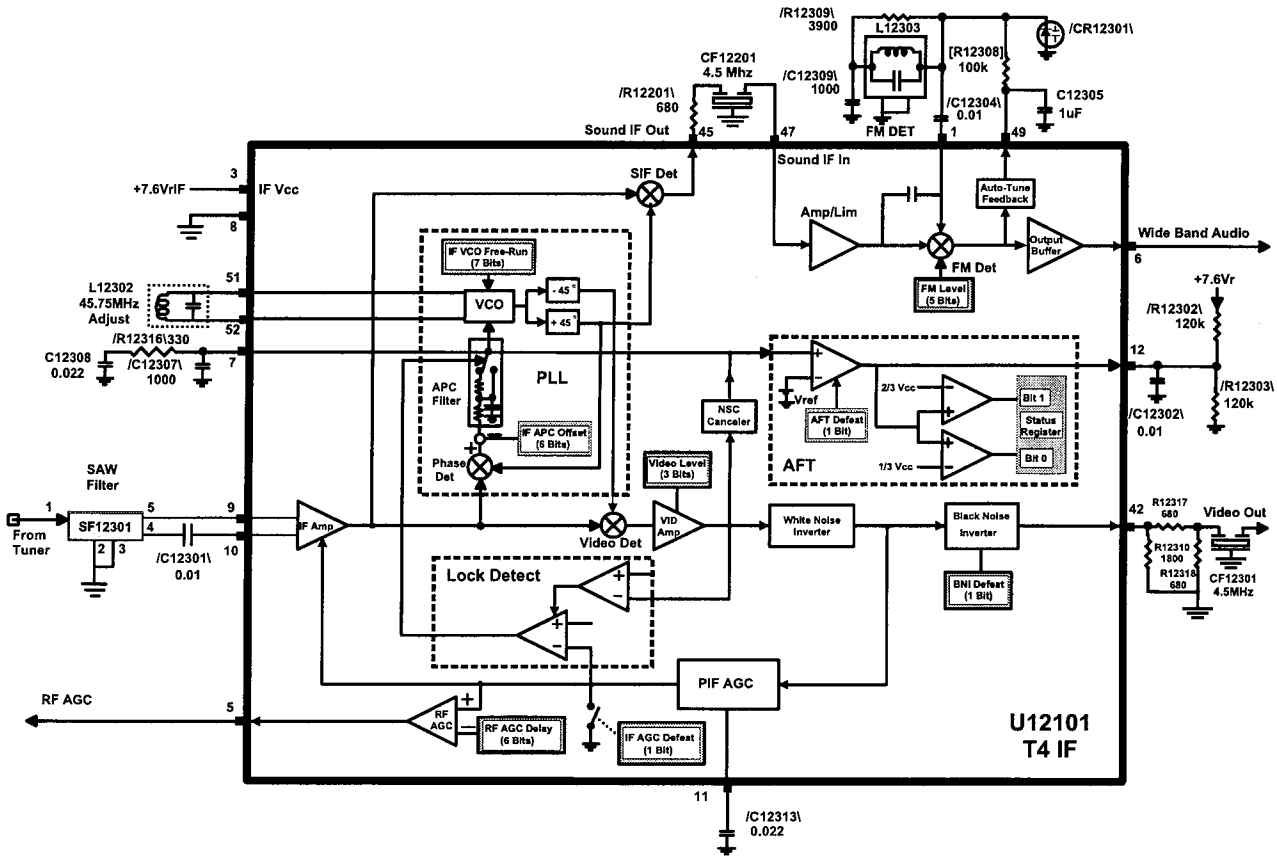


Figure 8-1, IF Circuitry

Overview

The IF circuits built into U12101, T4-Chip, and its associated circuitry provide:

- The majority of the desired channel selectivity.
- Automatic Gain Control (AGC) of the RF and IF amplifiers to optimize Signal to Noise (S/N) rejection and distortion.
- Automatic Fine Tuning (AFT) detection and feedback.
- Demodulation of the desired channel's audio and video bandpass signals.

The Picture IF (PIF) and Sound IF (SIF) functional blocks are all a part of the T4-Chip, U12101 with the exception of a 4.5 MHz Ceramic Band Pass Filter (BPF), CF12201, in the SIF channel and a 4.5 MHz ceramic sound trap, CF12301, in the Video output signal.

The 45.75MHz IF signal from the tuner is applied to the input of an intercarrier type Surface Acoustic Wave (SAW) filter, SF12301. The SAW filter has a Nyquist slope, a 41.25 MHz sound shelf, adjacent pix and sound trap, and Educational FM rejection.

SAW Filter

A SAW Filter (*S*urface *A*coustic *W*ave Filter) uses piezoelectric effects in a solid propagation medium to convert electrical signals to mechanical signals, tiny acoustic waves. The acoustic waves travel through the medium to the output where they are converted back to electrical signals. Controlling the properties of the medium can be used to make frequency specific control components such as filters. The medium is used for sorting signals by frequency. Its advantage over traditional BPF technologies is size and stability under harsh environments.

The output of the SAW filter is applied directly to the differential IF input of U12101 pins 9 & 10. The signal is amplified by a 3-stage variable gain IF amplifier and then split into the PIF and SIF channels.

Picture IF

Video detection is accomplished using a PLL system to remove the 45.75MHz IF carrier. The PLL has 2 IIC bus controls. One controls the VCO free running frequency and the other provides an offset for the Automatic Phase Control (APC). The PLL loop has sufficient bandwidth to eliminate tuner Local Oscillator (LO) phase noise.

Following the video detector, the video signal is put through a white noise and then black noise inverter for impulse noise immunity. The composite video signal is output at pin 42. The sound signal is then filtered from the composite video by CF12301, a ceramic 4.5 MHz sound trap.

The VCO control voltage from the PLL is also used for AFT detection. The control voltage is amplified and applied to a high and low comparator each with a 1-bit status flag. The status register flags are used to indicate when the AFT voltage is either below 1/3 the VCC level or above 2/3 the level of the VCC. The chassis microprocessor adjusts the tuner LO frequency then reads the AFT status register over the IIC bus, it attempts to center the LO to where neither status flag is HIGH. A PIF AGC loop is used to optimize the signal level in the IF amplifier and to generate an RF AGC voltage used to optimize the signal levels in the tuner.

Sound IF

The PLL VCO is also phase-shifted 90 degrees and used by the 1st SIF detector to down convert the 41.25 MHz sound carrier to 4.5 MHz. The 90-degree phase shift is also used to suppress video at the 4.5 MHz SIF output. The output of the 1st SIF detector is applied to the ceramic 4.5 MHz BPF, CF12201. A 4.5 MHz PLL FM detector, L12303 and associated circuitry, recovers the wide-band-audio signal (L+R, L-R, and SAP).

The FM Level is set over the I^2C bus and controls the WBA output amplitude by changing the current in the multiplier of the PLL. It may have "dead zones" at one or both ends of the control range where the PLL is unlocked and the output is essentially zero

The most important features of U12101 is that all IF alignments are electronically controlled over the IIC bus. The APC, VCO, Video, and RF AGC Delay alignments are the same as for the T-chip used in the CTC179/189.

F2PIP

Overview

In the following discussions, the larger on-screen picture will be referred to as the "main" picture and the small window will be referred to as the "PIP" picture.

The F2PIP is designed to provide a single moving picture-in-picture function. The PIP insert video source can be selected from several video sources. In addition, it provides a digital adaptive comb filter for the main picture Luma/Chroma (Y/C) separation. The F2PIP contains analog switches to perform the swap and overlay functions between tuner video, aux. video or two component (S-Video) sources. The module is controlled by the chassis main micro U13101 via I²C bus communications.

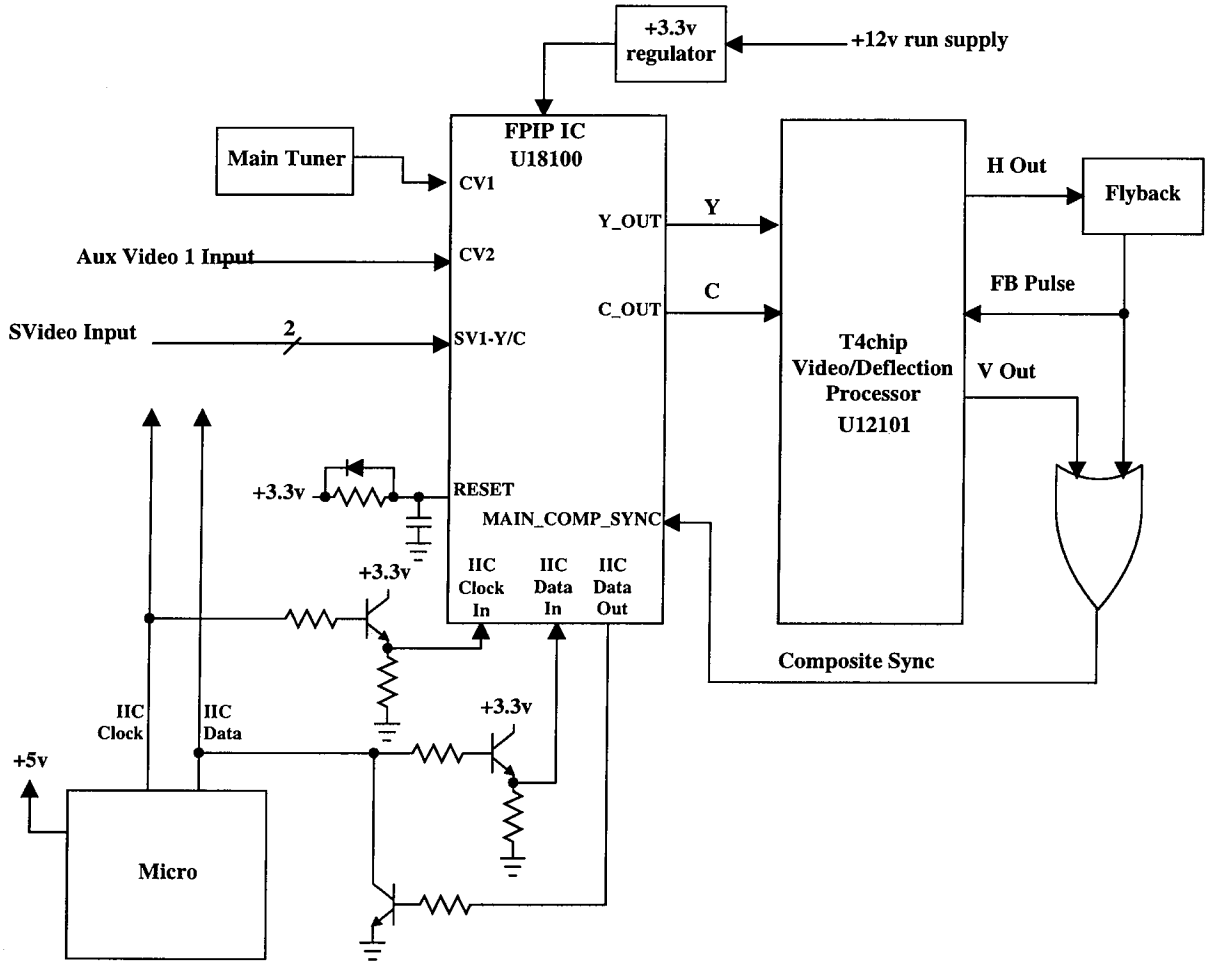


Figure 7-1, F2PIP Module Block Diagram

The module also contains audio jacks. The F2PIP module does nothing with these signals but routes them to the main chassis via input ESD networks and copper traces.

U18100

The F2PIP Module is built around the FPIP (Comb ***F***ilter/***P***ix-***I***n-***P***ix) CMOS IC U18100. This IC is designed to be a 1-chip solution for the single moving picture-in-picture function. The design of the F2PIP IC is intended to keep external components to a minimum. All inputs are designed to accept industry standard 1 volt (p-p) video sources (a 20% overhead is allowed), and all outputs are designed to provide industry standard 1 volt outputs. The F2PIP contains analog switches, (to perform the swap and overlay functions), A/D's (Analog-to-Digital converters), D/A's (Digital-to-Analog Converters), a crystal clock, and digital circuits necessary to process and control the PIP overlay picture.

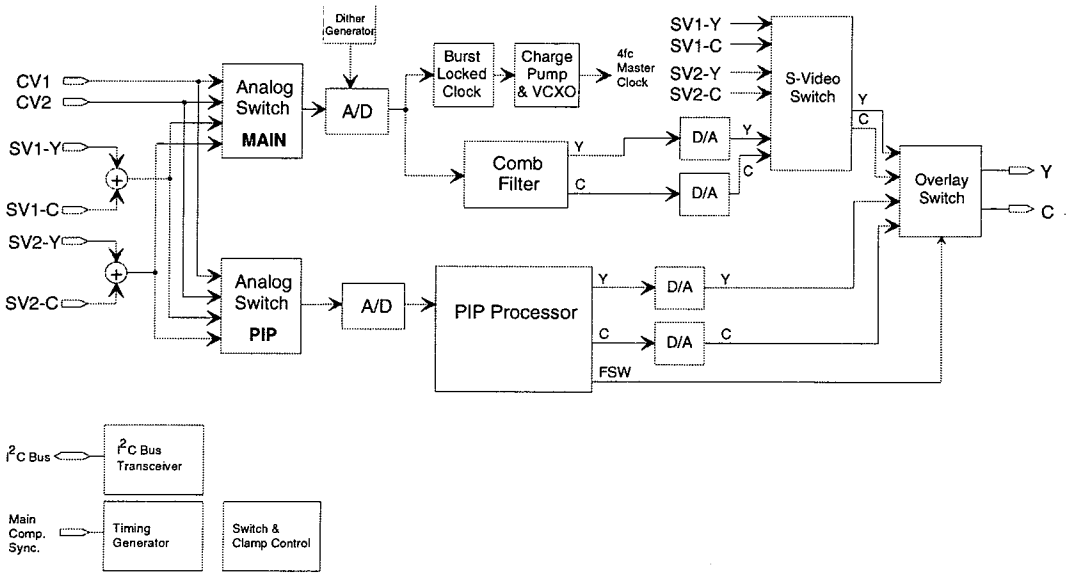


Figure 7-2, U18100 Top Level Block Diagram

The F2PIP is divided into several sections; analog switches, PIP processor, burst locked clock, adaptive comb, s-video switch and bus transceiver sections.

The *Analog Switches* are dual, 4 input switches. One is used to select the source of the main picture and the other to select the source of the PIP overlay.

The *PIP Processor* section includes a decode, encode and field RAM subsections. The decode subsection takes a composite video waveform and decodes it to Y, R-Y and B-Y for storage into the internal field memory. The encode subsection takes the information stored in the internal field memory and encodes chroma onto it, and then outputs separate Y/C signals for the PIP picture. These are combined to form a composite video signal for over-laying on the main composite video signal.

The *Burst Locked Clock* section generates the clock for the system. The BLC is locked to the color subcarrier of the main composite video signal.

The *S-Video Switch* selects between the comb filter's Y/C output or from 2 other S-Video Y/C sources. It then outputs the main picture Y/C. This is passed to the PIP overlay switch.

The *Bus Transceiver* section controls the F2PIP functionality. The registers that hold the control information are distributed throughout the IC.

IC Signal Processing

The IC can accept two composite video signals (CV 1 and CV 2) and two S-Video signals (SV1 and SV2) for pix-in-pix. One signal becomes the main picture and another of the sources can be used for the PIP picture (the same source can be used for both). The I^2C bus controls the source selection. These signals must be coupled with a capacitor to the F2PIP for the analog sync tip clamps to operate.

Analog Switches

The IC has two Analog Switches that select the main and PIP sources. Each analog switch has 4 inputs, main composite, aux. composite and 2 S-video Y/C inputs (only one is used). Once inside the IC, the S-Video luma and chroma signal are combined to form a third composite signal. The three composite video input signals are applied to the two analog switch circuits. The output of one switch is used for the main picture and the output of the other is used for the PIP picture. Any of the four inputs may be routed to either, or both of the outputs. The outputs of both analog switches are applied to 8 bit A/D (analog-to-digital) converters.

Main Signal Processing

The output of the analog switch processing the "main" signal is applied to the main A/D converter producing an 8 bit digital representation of the composite signal. The digital output is supplied to the Burst Locked Clock and the Line Comb.

Burst Lock Clock

The Burst Lock Clock provides a PIP ADC gain control signal to match PIP chroma amplitude to main chroma amplitude. It also generates the charge and discharge signals used to control the CHARGE PUMP VCXO (The VCXO is composed of an integrated Voltage-Controlled Phase-Shifter and an external crystal network). The charge and discharge signals are used to phase lock the VCXO output to the main picture burst. The charge pump charges or discharges the filter voltage proportionate to the phase error of the clock with respect to main picture burst.

Line Comb

The Line Comb filter separates the digital main picture luma and chroma information. The digital signals are converted back to analog signals by an 8 bit (luma) D/A converter and a 10 bit (chroma) D/A converter. The luma signal then exits the IC at pin 49 and is buffered by Q18108. It reenters the IC at pin 43 where it is applied to the S-Video switch. The main chroma signal exits the IC at pin 47 and is buffer by Q18107. It reenters at pin 45 and is also applied to the S-Video switch.

F2PIP PIP Processing

The output of the analog switch processing the "PIP" signal is applied to the PIP A/D converter producing an 8 bit digital representation of the composite signal. The digital output is supplied to the PIP Processor.

PIP Processor

The PIP Processor circuit separates the digital PIP picture luma and chroma information. It also produces a "Fast-Switch" signal derived from the sync. The

separate digital PIP luma and chroma signals are both converted back to analog via two 8-bit D/A converters. The D/A's have a current output. The reference for the current is provided internal to the F2PIP IC. The reference current for the chroma D/A varies with the amplitude of main video burst so that the chroma output will track the main video's chroma level. The luma D/A's reference is controllable in 64 steps via the I^2C bus. The analog PIP luma signal then exits the IC at pin 33, is buffered by Q18104 and reenters the IC at pin 35. The analog PIP chroma signal exits at pin 31 is buffered by Q18103 and reenters at pin 37. The PIP luma and chroma signals are then applied to the "Over-Lay" switch.

S-Video Switch

The S-Video Switch is used to select the source of the main picture. It chooses between the Y/C output from the Main Analog switch and the S-Video input at pins 3 and 5. The output of the S-Video switch always serves as the Main picture video and is applied to the Overlay Switch.

Overlay Switch

The Overlay Switch combines the analog luma and chroma (Y/C) signals of both the main picture and the PIP picture with the PIP signal overlaid on top of the main picture. This signal is then output at pin 39, luma, and pin 41, chroma. Q18105 and Q18106 buffer these signals. The buffered Y and C are sent to the T4 Chip, U16201 pins 38 and 40 for further processing.

Black Stretch Defeat

The output of pin 30 FSW T7 is used for Black Stretch Defeat. Whenever the PIP widow is active in the picture, pin 30 will have a pulse present. The pulse is buffered by Q18111 and output to the T4-chip, pin 37.

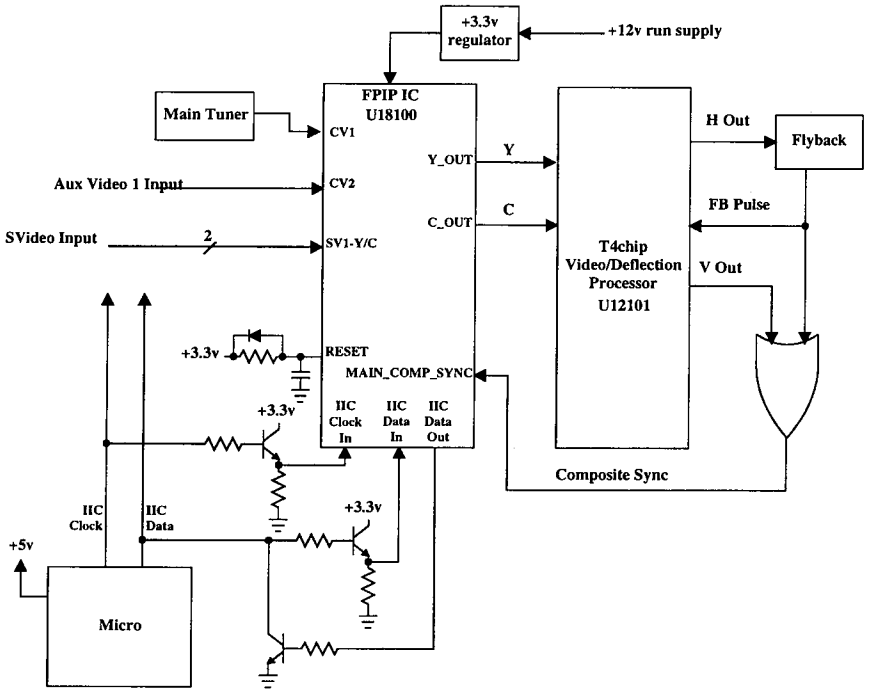


Figure 7-3, F2PIP Module Block Diagram

F2PIP Module Operation

Video Input Switching

The F2PIP module accepts composite video from the chassis tuner and has jacks for external S-video and Aux. composite video built onto the module. The module can use one or a combination of two of the sources to display PIP window within the main picture.

Zener diodes are attached to the aux. input at pin 1 and to the S-video Y/C inputs at pins 3 and 5 to prevent excessive video input levels or ESD from damaging the IC. The internal switching matrix is controlled via the I^2C bus from the System Control Microprocessor, U13101

F2PIP Module Inputs

Power Supply:

The F2PIP and associated circuitry operate on +3.3VDC. This supply is derived from the +12V supply by the 3-terminal regulator U18101. Considerable filtering exists between the regulator and the IC to reduce emitted radiation.

IIC Bus:

The F2PIP communicates to the chassis main micro via the I^2C Bus. The chassis I^2C bus operates on 0-5V pulses. Since the F2PIP IC operates on 3.3V, it needs a 0-3.3V bus. Therefore, the interface circuitry involving Q18100, Q18101, and Q18102 is needed. The F2PIP IC does not respond on the Clock line, therefore the interface is merely a buffer transistor (Q18100) with a voltage divider that reduces the pulse from 5V to 3.3V. The data bus is input to the IC through a buffer transistor (Q18101) with a voltage divider that reduces the pulse from 5V to 3.3V. The F2PIP must be able to talk on the Data line in order to send data. This is accomplished with a transistor Q18102 from the "Data Out" pin on the IC.

Composite Sync:

The F2PIP needs the sync information from the displayed main picture in order to be able to place the PIP picture properly. The sync information comes from the main chassis. The vertical pulse comes directly from the T4-chip. The horizontal pulse is derived from a flyback pulse off the IHVT. These 2 signals are clamped, conditioned and summed by Q18109, Q18110, Q18112 and Q18113.

Video Inputs:

The F2PIP is capable of accepting two composite video inputs and two S-Video inputs. One composite video input comes from the chassis tuner while the other comes from the Aux. Video 1 Input jack located on the module. The F2PIP module uses only one of the two S-video inputs the IC can handle. This S-Video signal comes from the S-Video input jack located on the module.

F2PIP Outputs

Y/C Output:

The module outputs luma and chroma signals for that are fed into the T4-chip to produce the RGB picture displayed on the screen.

Black Stretch Defeat:

The module outputs a signal connected to the Black Level Detector circuit of the T4chip. The signal is a pulse that is active when the PIP window is active. This signal is used to defeat Black Stretch in the portion of the picture where the PIP window is inserted.

Alignments

The following F2PIP alignments for the CTC203 can be adjusted using Chipper Check®.

- PIP Burst Gate
- PIP Comb D/A Alignment
- PIP Composite Video Chroma Alignment
- PIP Composite Video Tint Alignment
- PIP Contrast Alignment
- PIP S-Video Chroma Alignment
- PIP S-Video Tint Alignment

Troubleshooting

Symptom: Dead Set

1 Probable Cause: F2PIP 14.318Mhz oscillator not running. Probe U18100, pin 2, to check the oscillator. If it is within 1Khz of nominal frequency, the IC should run, talk to the bus, and make a reasonable main picture.

Symptom: No Main Pix

- Check the to see if the 3.3V supply is missing from one of the F2PIP IC pins.
- Check to see if IIC Bus communications is missing.
- Check Main Video signal path from the T4-chip.

Symptom: PIP will not turn on

- Check for proper vertical and horizontal pulses. Check for missing or incorrect sync at U18100 pin 24.

Symptom: PIP will turn on, but picture is black.

- Check PIP Video signal path from source to U18100.
- PIP Alignments are possibly wrong. Check PIP contrast and brightness alignments using Chipper Check™.

Symptom: PIP will turn on, but picture is distorted.

- Timing alignments are possibly wrong. Burst gate start and Back Porch Clamp will be in the wrong position if the Horizontal Offset correction number is not correct. Check alignments using Chipper Check™.

Video Processing

Overview

The video processing of the CTC203 chassis is similar to the processing in the CTC185 and CTC197. The CTC203 chassis uses the 4th generation T-chip for IF, audio detection, video processing, and deflection processing. As has been discussed earlier, the T4-Chip is an IIC bus controlled IC. Video picture adjustments are performed via OSD menu and include: color, tint, contrast ("picture"), brightness and sharpness. Individual set-up status includes only "autocolor" which is a menu toggle item. Customer settings of the various video parameters are stored in non-volatile memory, EEPROM U13102. Factory presets are also stored in the EEPROM and may be recalled by the "reset" function in the menu.

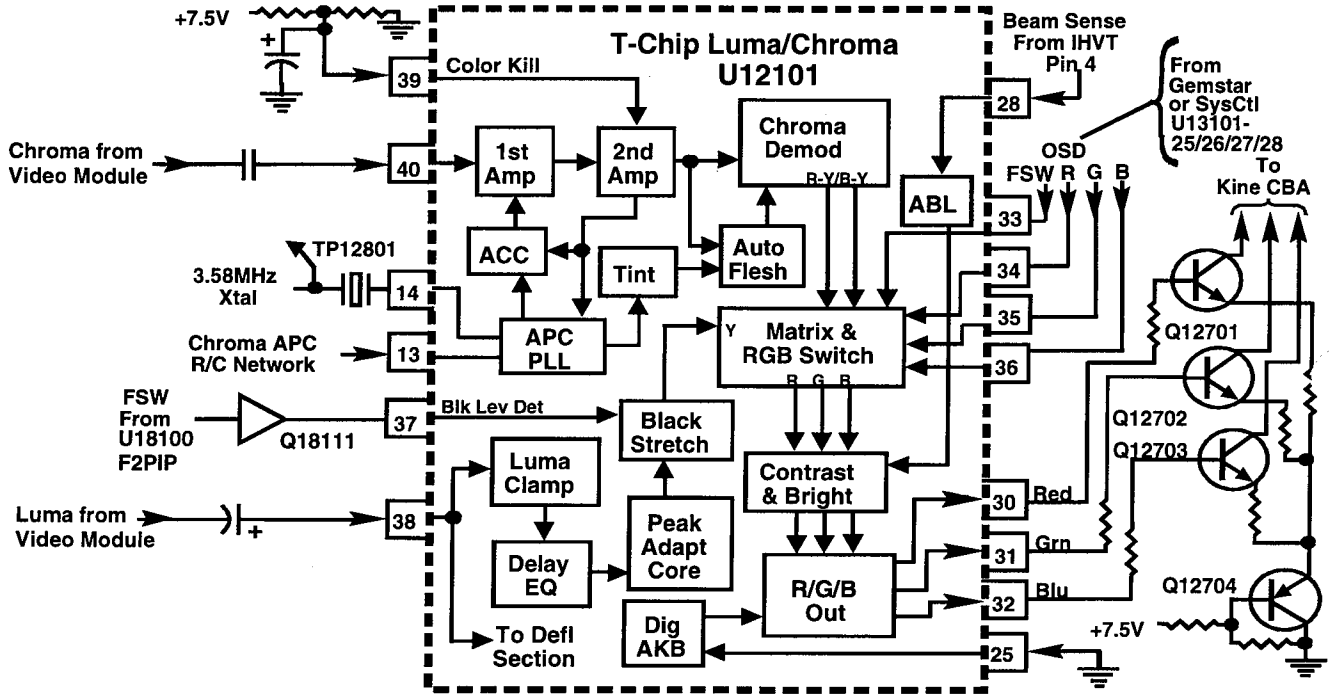


Figure 8-1, T-Chip Video Processing Block Diagram

Figure 8-1 is a block diagram of the video processing portion of U12101, T4-Chip. The video section of the CTC203 is composed of 4 main areas; luma processing, chroma processing, external RGB inputs, and RGB outputs. With only a few exceptions, all circuitry for these functions is contained in the T4-Chip. Composite video from the T4-Chip is sent to the "Video Module", either F2PIP, analog comb or video switching where the video signal is separated into separate Luma and Chroma signals and fed back to the T4-Chip.

Luma Processing

The Luminance section block diagram of the T4-Chip is shown in Figure 8-2 along with the RGB section. The luminance section video input is applied to pin 38, from a Luma buffer on the Video Module. The input to the luminance section of the T4-Chip is expected to be approximately 1 Volt sync tip to white. The signal at pin 38 is clamped to about 3.8 volts at sync tip, attenuated by 20dB and then filtered. Attenuation and clamping are done so that the filter section can operate linearly. Too much signal would send the filter into an area where the nonlinear characteristics would make the output slightly unpredictable. The filter section is bus controlled and can be switched between a 3.58 MHz notch (as used in the CTC-185 when no external Y/C separation is available), 4.6 MHz notch, and a 8.0 MHz all pass filter. The CTC203 versions having F2PIP or Analog Comb use the 8 MHz all pass filter. Using the all pass filter provides for maximum S-Video and Auxiliary Video bandwidth. Base chassis versions which are non comb utilize the 3.58 MHz trap to provide at least some Y/C separation. The CTC203 does not use the 4.6 MHz notch.

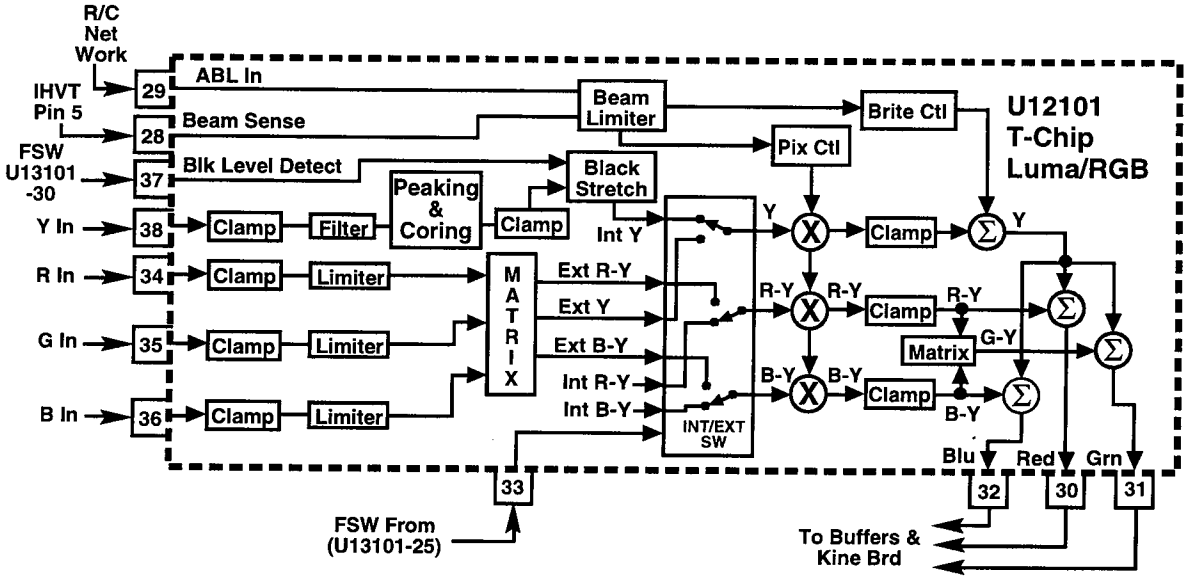


Figure 8-2, Luma/RGB Block Diagram

After filtering, the luma signal is once again clamped, and passed through the black stretch circuitry Figure 8-3. This circuit modifies the video transfer function to enhance contrast on low APL scenes. Black stretch operates selectively on the luma level and is disabled in the PIP window. Black stretch is a duty cycle dependent non-linear black level processor. It attempts to maintain a consistent black level in the displayed picture. Black stretch looks for low duty cycle black signals. If the blackest information within the duty cycle is on the order of 15 IRE or less, black stretch will attempt to stretch that signal toward black of about 2 or 3 IRE.

The duty cycle is set by C12702 and R12703 at the Black Level Detector, pin 37 (Figure 8-3). The normal operating voltage is about 4.6VDC. Black Stretch is defeated by pulling the voltage at pin 37 down. The F2PIP module supplies a signal during PIP to defeat black stretch.

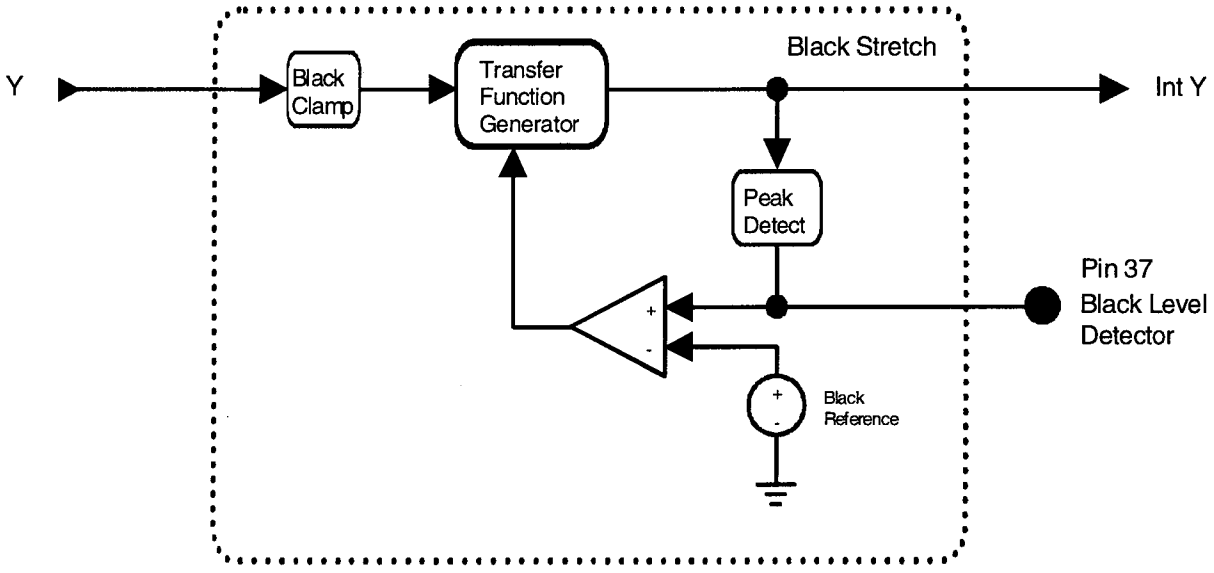


Figure 8-3, Black Stretch

Chroma Processing

Chroma processing in the CTC203 is similar to the CTC197 in that the T4-Chip can receive separated Y/C signals from the Video Module, either the F2PIP or Analog Comb module. In Base chassis versions Chroma processing is similar to the CTC185 in that both the Y and C inputs of the T4 are driven from a common source. The chroma section expects to get a signal at pin 40 whose amplitude is approximately 290 mV peak to peak burst. The chroma signal is high pass filtered by C12805 and R12805 (Figure 8-4) to remove low frequency luma that would affect the DC dynamic range of the first chroma amplifier.

The chroma section includes a filter that is configured as either a symmetrical filter (used for aux. input and S-video mode) or peaker (used for turner/if operation). The filter is IIC bus controlled and can be bypassed. The filtered chroma signal is routed through the overload amp and then on to the 2nd chroma amp stage. The 2nd chroma amp stage is made up of two identical amplifiers in parallel. The "B" amp output drives the chroma overload detector that controls the overload amp gain. This forms a low gain AGC circuit that attempts to maintain the average chroma saturation

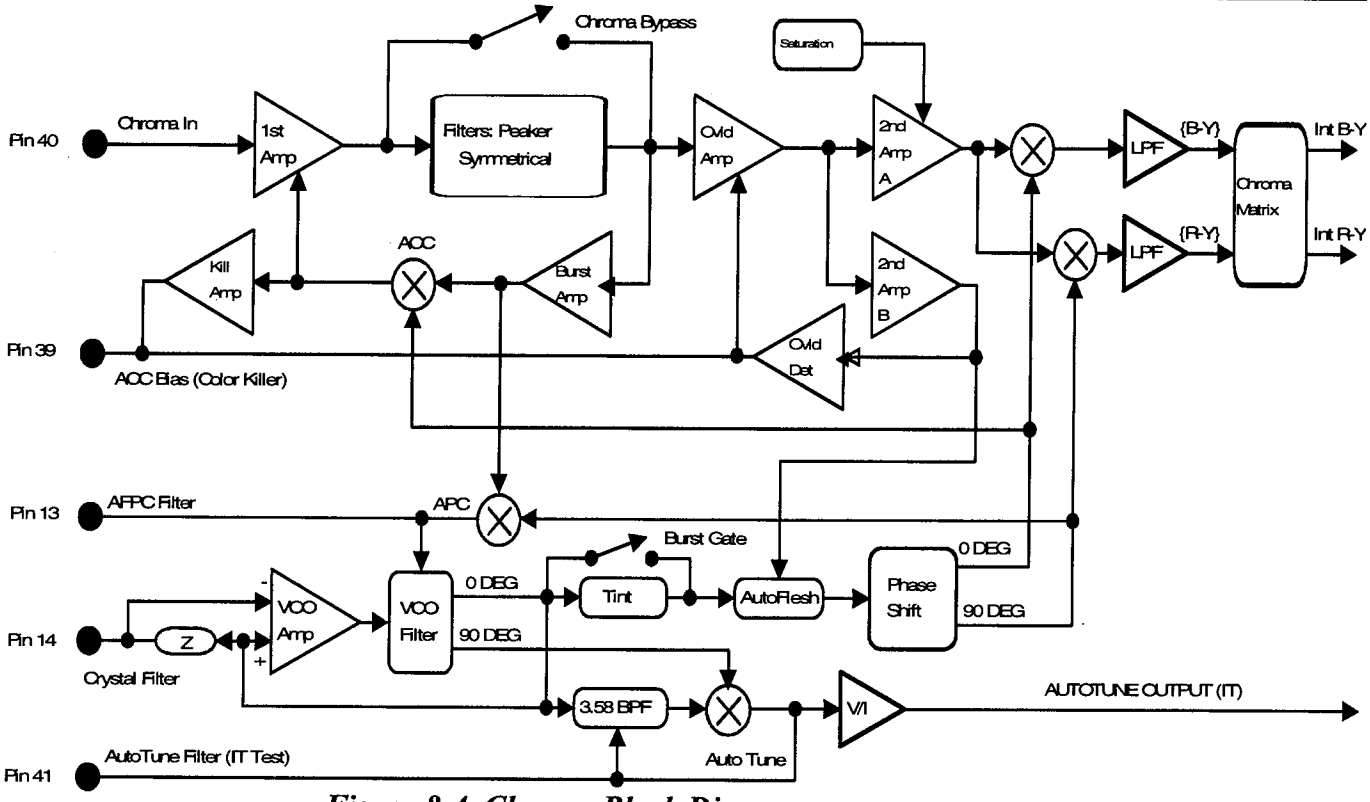


Figure 8-4, Chroma Block Diagram

within some prescribed limits. Chroma overload is enabled over the IIC bus. Chroma saturation is applied to the 2nd chroma amp "A", and then the demodulator inputs. The demodulator's output is applied to lowpass networks to reduce demodulator artifacts. The chrominance block also includes a VCO, ACC (Automatic Color Control), Auto tune Loop, APC (Automatic Phase Control), Color Killer, and Auto Color.

The VCO is the heart of the chroma system. It is a single pin design that uses a 3.58 MHz crystal oscillator. A filter consisting of a 3.58 MHz series resonant crystal (Y12801) is connected to ground through a series RC, (R12803 and C12803), at pin 14. At the resonant frequency of the series filter, positive feedback is generated sustaining oscillation. The VCO filter is then tuned to match the frequency of the incoming burst signal. The output of the VCO goes through a filter whose outputs are 0 degrees and 90 degrees out of phase with the input signal. The 0 degree output drives the tint control and autoflesh stages, and the 90 degree output is used to drive the autotune section

The ACC (Automatic Color Control) detector monitors the burst amplitude at the output of the filter section and adjusts the 1st chroma amplifier gain to maintain a constant level. The output of the ACC is compared to a kill threshold reference in the color killer amplifier. If the detected burst amplitude is below approximately 2.4 IRE, the killer is activated, shutting down the overload amplifier. Voltage on Pin 39 is about 1.5V if no chroma is available. Pin 39 will be about 3.8V for normal operation.

The Autotune loop compensates for effects of processing on the integrated filters. Auto tune works by making a phase comparison of the 90 degree output of the VCO and the VCO amplifier input after the 3.58 MHz bandpass filter. If the resonant frequency of the bandpass is not correct, the auto tune detector sees the error and supplies a correction voltage. It attempts to tune the bandpass such that the center frequency of the bandpass will be equal to the center frequency of the chroma oscillator. The output of the Autotune loop is a current (I_T), which is used to tune the chroma bandpass filter. Additionally, the scaled auto tune output is sent to every filter on the IC. The Autotune loop has an external filter (C12704 and R12705 Figure 8-6), on pin 41 (TEST_IT FILTER). The nominal voltage on pin 41 is about 5.5VDC.

The APC, (Automatic Phase Control) provides an accurate tracking of the burst phase, which is always at 180 degrees reference. The APC Filter, pin 13 has an external circuit consisting of an R-C time constant C12806 and R12808 (Figure 8-6), and 5 VDC bias voltage source formed by the R12806, R12907 divider. The nominal voltage on pin 13 is about 5.5 VDC.

The Color Killer is accomplished by taking the output of the ACC detector and comparing it to a reference in the killer amplifier. If the detected burst amplitude is below approximately 2.4 IRE the killer is activated. When the killer is active the voltage at pin 39 is pulled to about 1.5 VDC.

Auto-color is a combination of two features, chroma overload and autoflesh. Auto-color is enabled over the IIC bus. In the Autoflesh block, a phase detector compares chroma from the output of the 2nd chroma amp "B" section to the subcarrier from the tint control. When the incoming chroma phase is in the vicinity of "flesh tone" (approximately 123°, dependent on the customer tint setting), a phase correction is applied to the subcarrier to move it back towards the "flesh" setting.

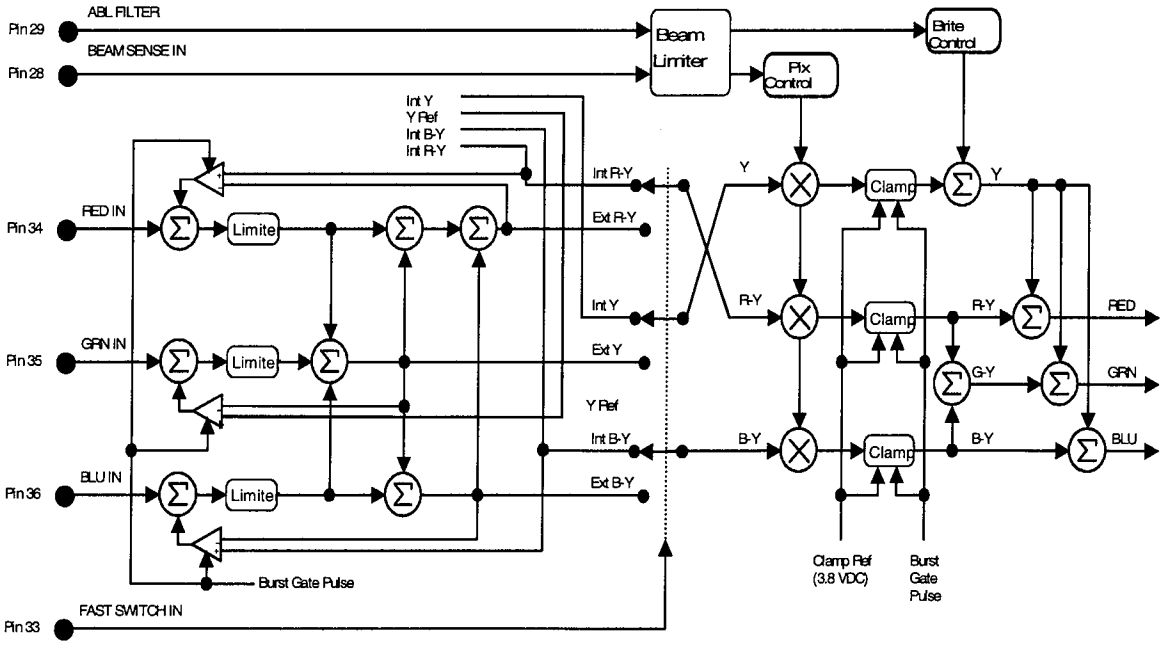


Figure 8-5, T4-Chip RGB Block Diagram

RGB

Figure 8-5 is the block diagram for the RGB section of the T4-Chip.

External RGB Input Processing

The external RGB inputs are used for OSD (On Screen Display) processing for the CTC203. OSD signals from the microprocessor and Gemstar module are applied to the external RGB inputs (pin 34, 35 & 36, through input clamp capacitors. The signals are limited at approximately 700mVpp (corresponding to 100 IRE). In the CTC203 the input drive level will be somewhat less than this, typically in the range of 70 IRE or 500 mVpp. Signals are de-matrixed into luminance(ExtY) and Ext R-Y and Ext B-Y

RGB Internal/External Switching

Selection of either External RGB (OSD) or Internal RGB (video) is accomplished with the int/ext switch. The internal and external video signals are applied to the int/ ext switch. The switch selects between the signals depending on the voltage at the fast switch input, pin 33. Any voltage above approximately 0.7 Volts will select the external RGB (OSD) signals. After the switch, the selected signals go to the interface and output sections.

RGB interface and Output Section

The RGB interface is a level control and matrix section. The Pix Control or Contrast control adjusts the gain of the Y, R-Y and B-Y amplifiers and varies the black to white signal amplitude at the RGB outputs. It has an adjustment range of about 10dB. The signals are then clamped. R-Y and B-Y are matrixed to obtain G-Y, and then the three color difference signals (R-Y, G-Y & B-Y) and luminance (Y) are matrixed to obtain Red, Green, and Blue component signals. The Brightness Control adjusts the level of the luma signal (Y) that adjusts the black level of the signals at the RGB outputs. This raises the DC level of these signals. The Brightness Control has a range of about ± 20 IRE. A typical RGB output, pins 30, 31, and 32, will have a black level of about 2.65VDC and a peak black to white voltage of about 2 Volts for a non beam limited 100 IRE pulse at maximum contrast. Blanking has been inserted at this point and the blanking portion of the signal should extend down to about 1 volt. These signals are used to drive the kine circuitry.

RGB Output Section

After source selection, the pix control (picture control) adjusts the amplitude of the Y, R-Y, and B-Y signals. These are then clamped and the brightness control is applied to the Y signal. R-Y and B-Y are matrixed to form an additional signal, G-Y, and the Y component is summed with all three color difference signals to form Red, Green, and Blue component signals

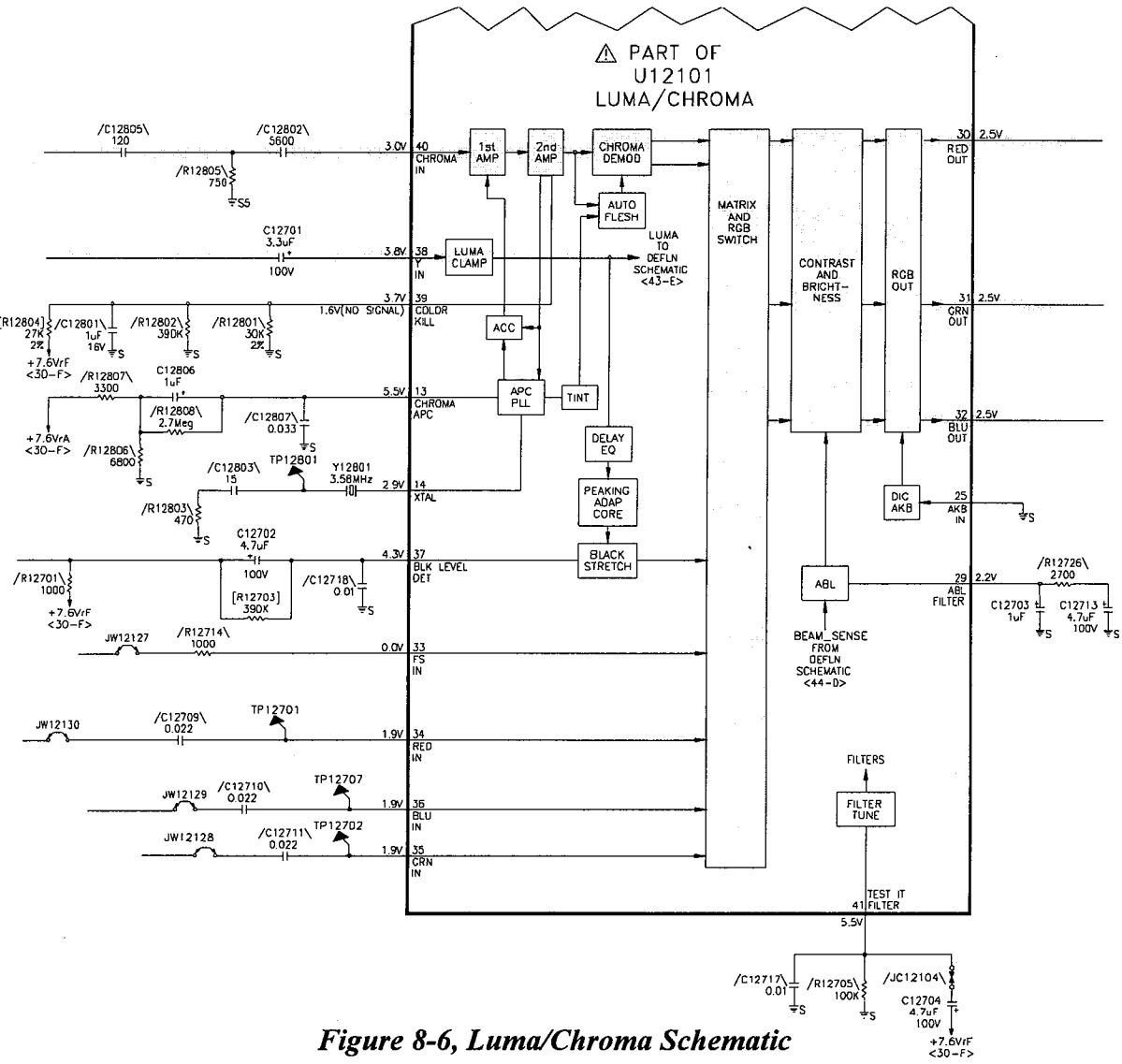


Figure 8-6, Luma/Chroma Schematic

Troubleshooting Luma/Chroma

No Luminance

1. Check the brightness and contrast controls from the user menu.
2. Check the input signal at U12101 pin 38. It should be approximately 1Vp-p, sync to 100 IRE.
3. Check the beam limiter control voltage at pin 28. The circuit is active below 6 volts.
4. Check the Fast Switch input at pin 33. A voltage greater than 0.7 volts will blank the video to let OSD through.

Color problems can best be diagnosed using an oscilloscope and a digital voltmeter.

No Chroma

1. Check the Color and Tint controls from the user menu.
2. Check the chroma input level at U12101 pin 40. It should be approximately 300 mVp-p.
3. Defeat the Color Killer circuit by applying approximately 4 volts DC to pin 39 of U12101. Free running chroma should be viewable on the screen (barber pole) if the 3.58 MHz oscillator is running.

Autocolor / Autoflesh Confirmation

Turn Auto color on and off from the video menu while viewing an NTSC color bar signal.

- The magenta bar should shift towards red.
- Chroma saturation should reduce slightly.

Note: The value of the resistors connected to U12101 pin 39 (R12804, R12802 and R12801) are critical for proper color saturation

CRT Management

The T4-Chip also supplies low level signal processing for CRT management functions including black level and beam limiting. Like the CTC185 the CTC203 does not utilize the AKB function of the T4-Chip.

Beam Current Limiting

The beam limiter addresses the picture control as well as the brightness control inside the T4 video processing circuits, Figure 8-5. Beam current is sensed by pin 28 monitoring the secondary winding of the IHVT that supplies beam current. Normal beam limiting is accomplished by reducing contrast. However, if black level is adjusted too high by the consumer controls, and beam limiting is called for, the brightness control reduces the Y level first, without moving the consumer OSD. If insufficient beam current reduction is not achieved, the limiter can go into emergency brightness reduction. In this mode, the brightness is reduced to a very low level (it can be reduced to almost black). The beam limiter threshold is primarily set by R14706. The voltage on the beam sense pin, pin 28 approaches 7.5 VDC at zero beam and 6 VDC at maximum beam. An ABL (Automatic Brightness Level) filter on pin 29 sets the response time of the ABL circuit. Normally beam limiting will begin within 30 to 40 horizontal lines.

CRT Drivers

General

The CRT drive amplifiers receive the RGB signals from the T4chip and amplify them to drive the CRT cathodes. The amplifiers are capable of outputting approximately 150Vp-p with a bandwidth of approximately 5Mhz. The CTC203 chassis uses cascode amplifiers to drive the CRT Figure 8-7. This is a change from product like the CTC187 and CTC185 that use a single transistor in common emitter configuration. The cascode circuit is not new, however. The circuit used in the CTC203 is basically the same as the CTC169 or a simplified CTC197.

Circuit Description

The cascode configuration is a 2 transistor amp with the input transistor connected as a common emitter and the output transistor connected as common base. The signal enters the base of the lower transistor and exits the collector of the upper. The collector current of each transistor is approximately the same. However, the voltage Vce of each device is greatly different. The upper device can have Vce of up to 120V. The lower device can have Vce max of only 12V. Therefore, the power in the upper device can be 10 times that of the lower.

The schematic Figure 8-7 shows the circuitry for the CRT driver circuit. This circuit is split between the main circuit board and the CRT socket board. For this discussion, we will consider only the green channel. The Red and Blue are identical circuits.

The emitter of Q12704 forms a 'virtual ground' where the currents from all three outputs return. This transistor provides an AC ground that is not 0VDC. This is desirable in order to bias the circuit correctly. Changing the DC voltage on the base of Q12704 changes the DC voltage at the collector of Q15102. The emitter of Q12704 is one junction drop above the base divider voltage. The value of R12713 is different for different size picture tubes. This is because the VLS tube operates with G1 at 20VDC while at smaller screen sizes G1 is grounded. This means for a 150Volt cutoff (Vcuttoff-VG1), black must be at 170Volts. In the grounded grid versions, black is at 150Volts.

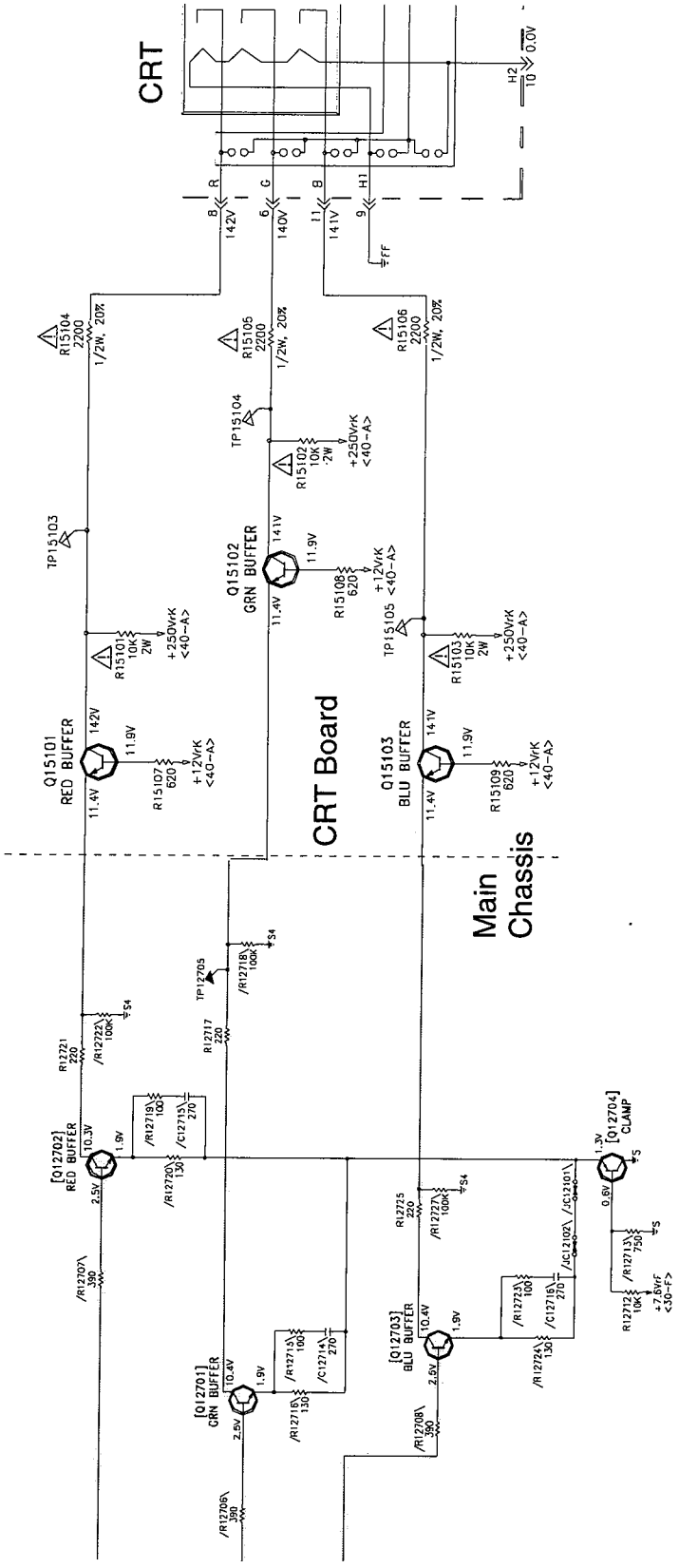


Figure 8-7, CRT Driver Schematic

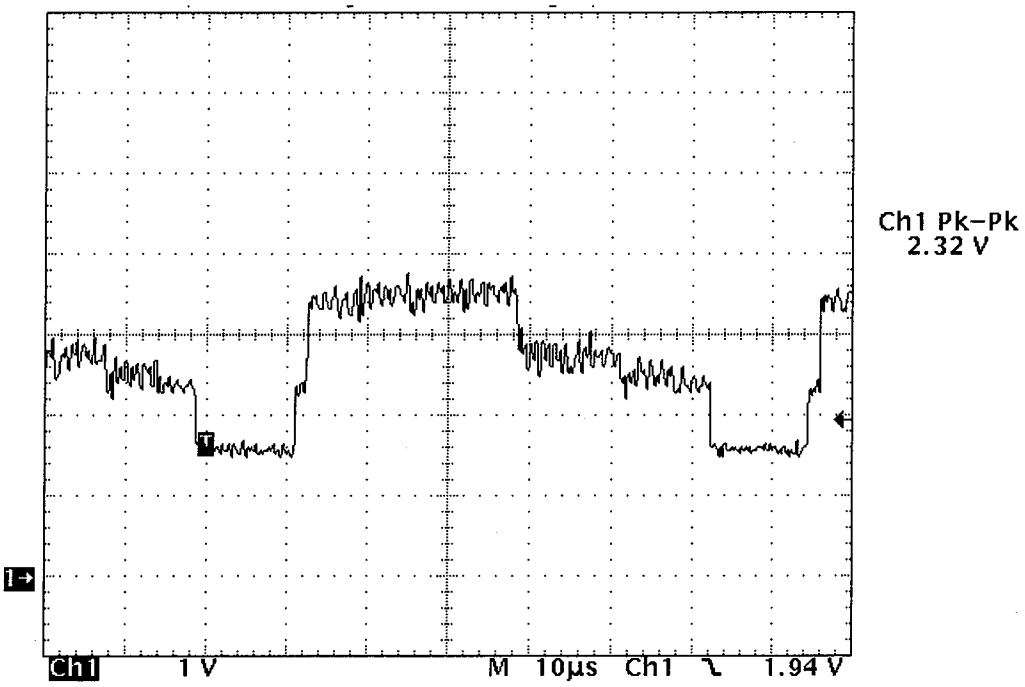


Figure 8-8A, Q12701-B

The green signal is output from pin 31 of the T4 and applied to the base of Q12701, Figure 8-8A. As the signal decreases, Q12701 is less forward biased reducing the collector current. This causes the current in Q15102 to decrease causing the collector voltage to increase, Figure 8-8B. As the signal increases, the collector voltage of Q15102 begins to increase towards the collector supply voltage, +250V. This is also the cathode voltage for the green gun of the CRT. Note that as this signal increases, it is actually moving towards the blanking pedestal, or black. Beam current in a CRT is proportional to the bias voltage between the cathode and the screen grid. As bias voltage decreases, beam current decreases. Since the screen grid is normally fixed at around +300–400 volts, as the collector voltage tracks towards the power supply voltage of +250V, bias decreases, decreasing beam current.

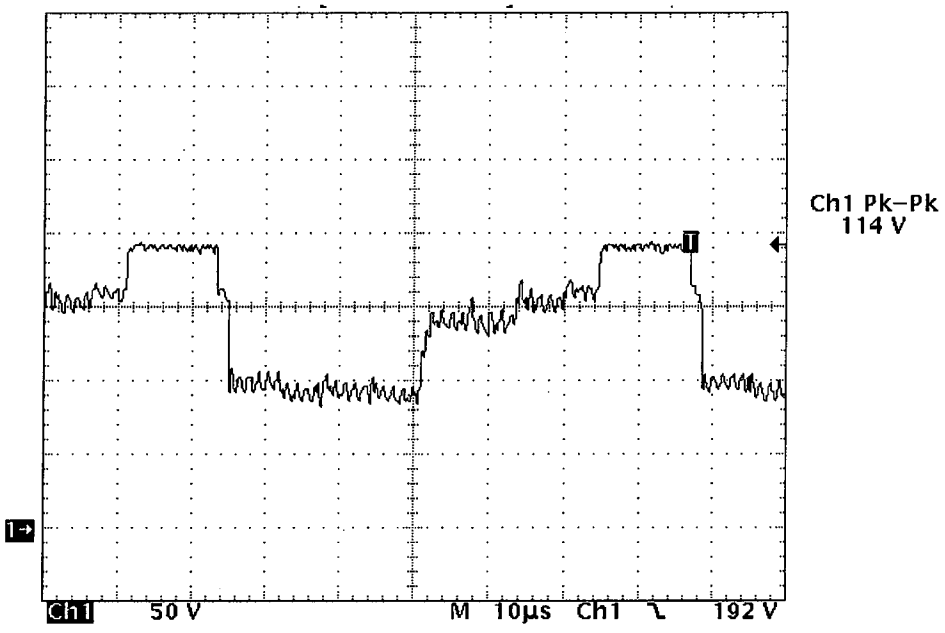


Figure 8-8B, Q15102-C

R15102 is the load resistor for the amp. This resistor limits the power in Q15102. Its value is selected so that the output transistor, Q15102, runs at optimum power dissipation and bandwidth. R15105 is the "flashover" resistor that limits the current from the CRT in case of internal arc. R15108 connects the +12V bias to the base of Q15102 and also limits the base current. This helps reduce the possibility of saturation. R12718 serves to keep Q15102 turned on slightly even during blanking. This decreases the RFI generated from switching the transistor completely off and back on. Its effect can be seen by comparing the voltage at blanking to the level of the CRT supply. Without this resistor, blanking level would be at the supply voltage. R12717 is used to limit the current into Q12701 in case of CRT arc. R12706 is used to protect the T4chip from ESD and CRT arcs. R12716 along with R15102 determine the gain of the amp. This 10K/130ohm combination is the same that is used in CTC187. R12715 and C12714 provide some peaking and extend the bandwidth of the circuit. This is accomplished by effectively reducing the value of R12716 as the frequency increases.

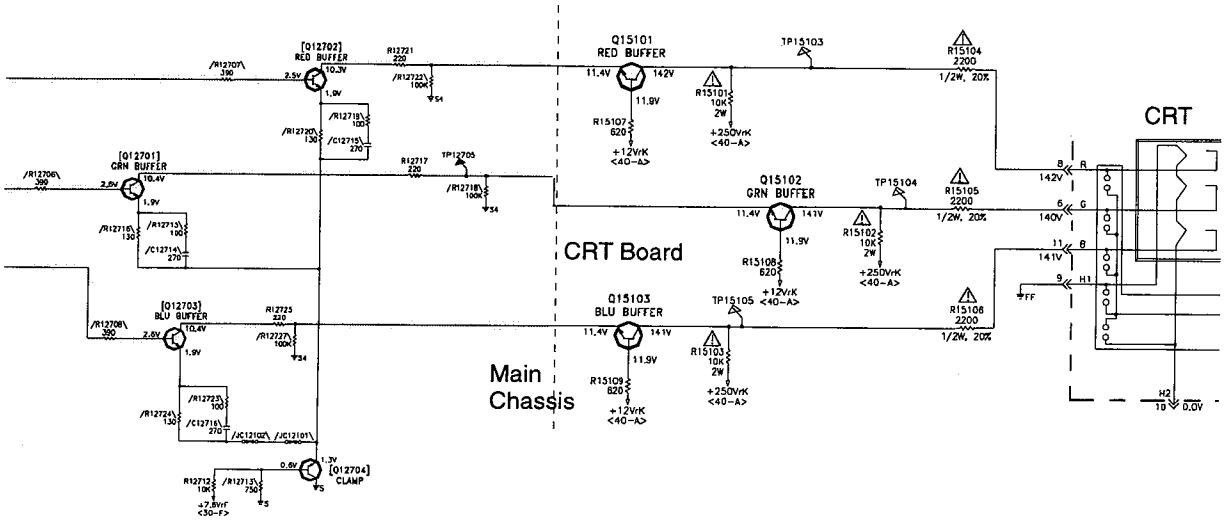


Figure 8-7, CRT Driver Schematic (Repeated)

CTC203 Video Module

Overview

The CTC203 chassis has been designed so that feature difference between models is accomplished for the most part by the use of different flavors of the Video Module. Figure 8-9 is a block diagram of the CTC203 Video System. The video module can have various numbers of external jacks for Audio, Composite Video and S-Video. The video module will be one of the following, Analog Comb, F2PIP, Video Switch or just as a video feed through for 0 jack models.

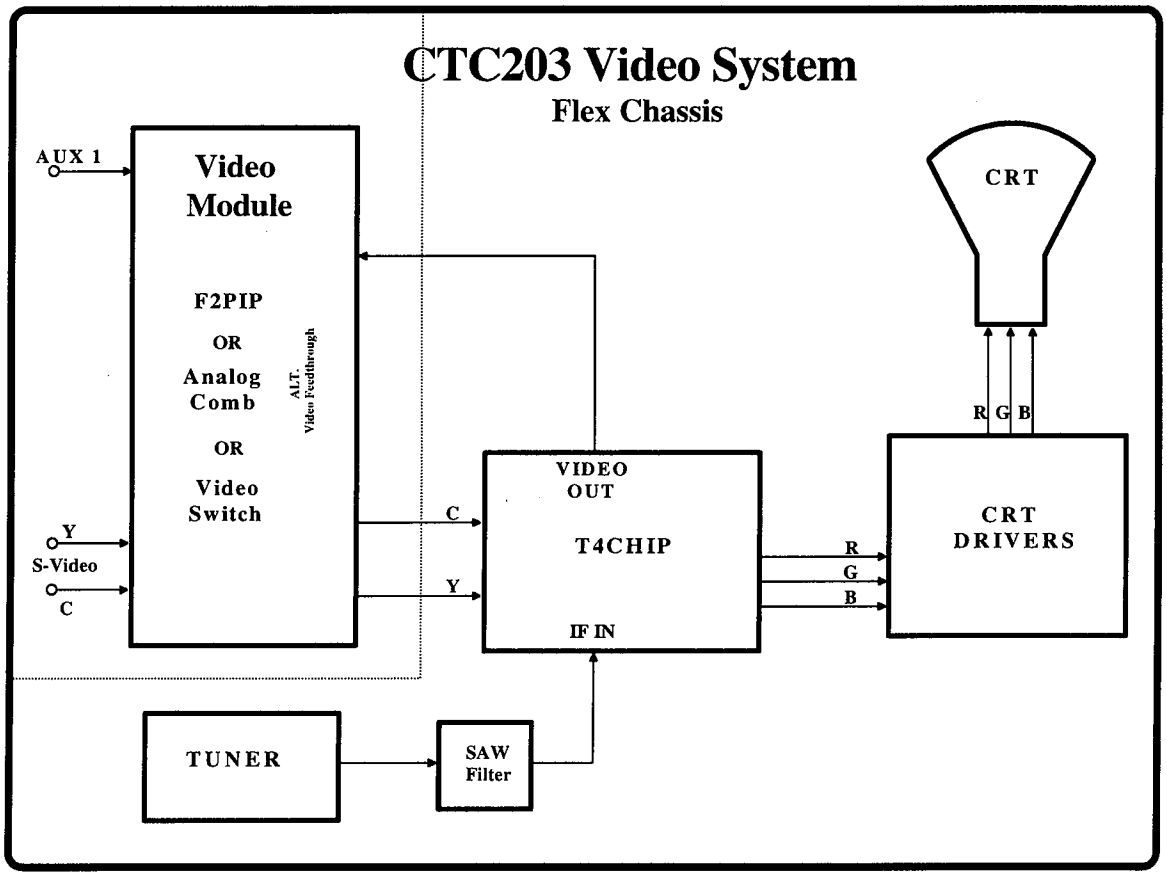
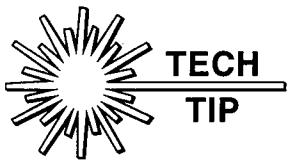


Figure 8-9, CTC203 Video Block Diagram

Regardless of the configuration, the video module uses the same connectors to the main circuit board for all applications. The connecting interface on the main chassis is identical for all modules although not all signals are used on all configurations. The chassis will work with any module connected.



If the Video Module is removed the instrument will not produce a picture. To troubleshoot the instrument without the Video Module jumper pin 8, J12101, to pins 5&6, J12101. This connects the buffered TV Video output from pin 42 of the T4 to the Y/C inputs, pins 38 & 40.

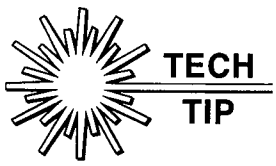
Module Inputs

+12V:

The +12V run supply is provided to the modules. The modules can use the +12V run to derive their specific voltage needs.

Ground:

The main chassis ground reference.



TV Video:

The main composite video from the T4-chip.

Composite Video Switch:

Logic line from U13101 used to switch between composite main and aux video on the analog comb.

Comb S-Video Switch:

Logic line from U13101 used to switch between comb Y/C and S-video Y/C on the analog comb.

IIC Bus:

The main chassis communicates to the modules via the IIC Bus. The chassis IIC bus operates on 0-5V pulses. Only the F2PIP module uses the IIC bus.

Vertical Sync:

Vertical sync pulse from deflection, used by the F2PIP module for positioning the PIP picture.

FP (Flyback Pulse):

Horizontal sync pulse from the IHVT, used by the F2PIP module for positioning the PIP picture.

Module Outputs

Chroma (C):

The Chroma signal to the T4-chip.

Luminance (Y):

The Luminance signal to the T4-chip.

Black Stretch Defeat:

This signal is only output from the F2PIP and connects to the Black Level Detector circuit of the T4-Chip. The signal is a pulse that is active during the PIP window time. This signal is used to defeat Black Stretch inside the PIP window.

T4-Chip U12101

T-Chip Overview

The CTC203 chassis uses the latest 4th generation in a series of television specific "Thomson one-chip" IC's designed to perform most low level signal processing in a television chassis. This one-chip combines all the functions required for an NTSC color TV system. A block diagram is shown in Figure 9-1. Included functions are:

- Pix IF with analog AFT
- Sound IF and FM demodulator
- Audio volume control
- Video processing with bus selectable on-chip lowpass filters
- Chroma processing with bus selectable on-chip bandpass filters
- Horizontal and vertical deflection with east / west parabola generator
- External RGB switching
- Digital AKB circuitry
- Bus control of all customer controls and factory alignments

The T4-Chip is compatible with the Philips Inter IC (IIC) bi-directional 2-wire serial data communications bus.

T4-Chip Bus Specifics

This section is a general overview of the IIC bus standard and not intended to be a detailed description. It will focus on the bus structure and video processing performed by the T4. Within the IIC bus definition, the T4-Chip is considered to be a slave-only device. This is because the IC cannot initiate a data transaction but can only respond to commands from an IIC bus master device such as the chassis microprocessor. The T4-Chip bus transceiver supports only one write mode and one read mode.

POR (Power-On Reset) Operation

The T4-Chip includes a standby power supply monitor referred to as the POR. This circuit detects when the Standby Vcc (+7.6Vs) voltage has dropped below the normal range and shuts the IC off by stopping the horizontal output. The output of the POR circuit is available to the micro for status control. The POR circuit output is latched and will reset only with an OFF to ON transition of the ON/OFF bit. This means that when a television is ON and a Standby Vcc transient occurs, triggering the POR circuit, it is necessary to send an OFF command, followed by an ON command in order to get the set started again. If the Standby Vcc is still too low when an ON command is received, the IC will stay in the OFF mode and the process must be repeated.

Bus Transceiver Reset

The T4-Chip bus transceiver contains an internal reset circuit sensitive to the Standby Vcc level. This reset circuit is separate from the IC's Power-On-Reset (POR) circuit and is designed to keep bus communications active at Standby Vcc levels that may be lower than normal. POR occurs at +6.3 volts while the bus transceiver will remain operational to Standby Vcc levels as low as +2.5 volts. When a bus transceiver reset is detected the circuit enters an idle mode in which SDA (Data Bus) is left high and bus communications are ignored. When the Standby Vcc is lower than normal but above +2.5 volts, the bus transceiver will remain operational. However, the saturation voltage of the SDA line is not guaranteed. Both the SDA and the SCL (Bus Clock) lines are internally clamped to Standby Vcc via protection diodes.

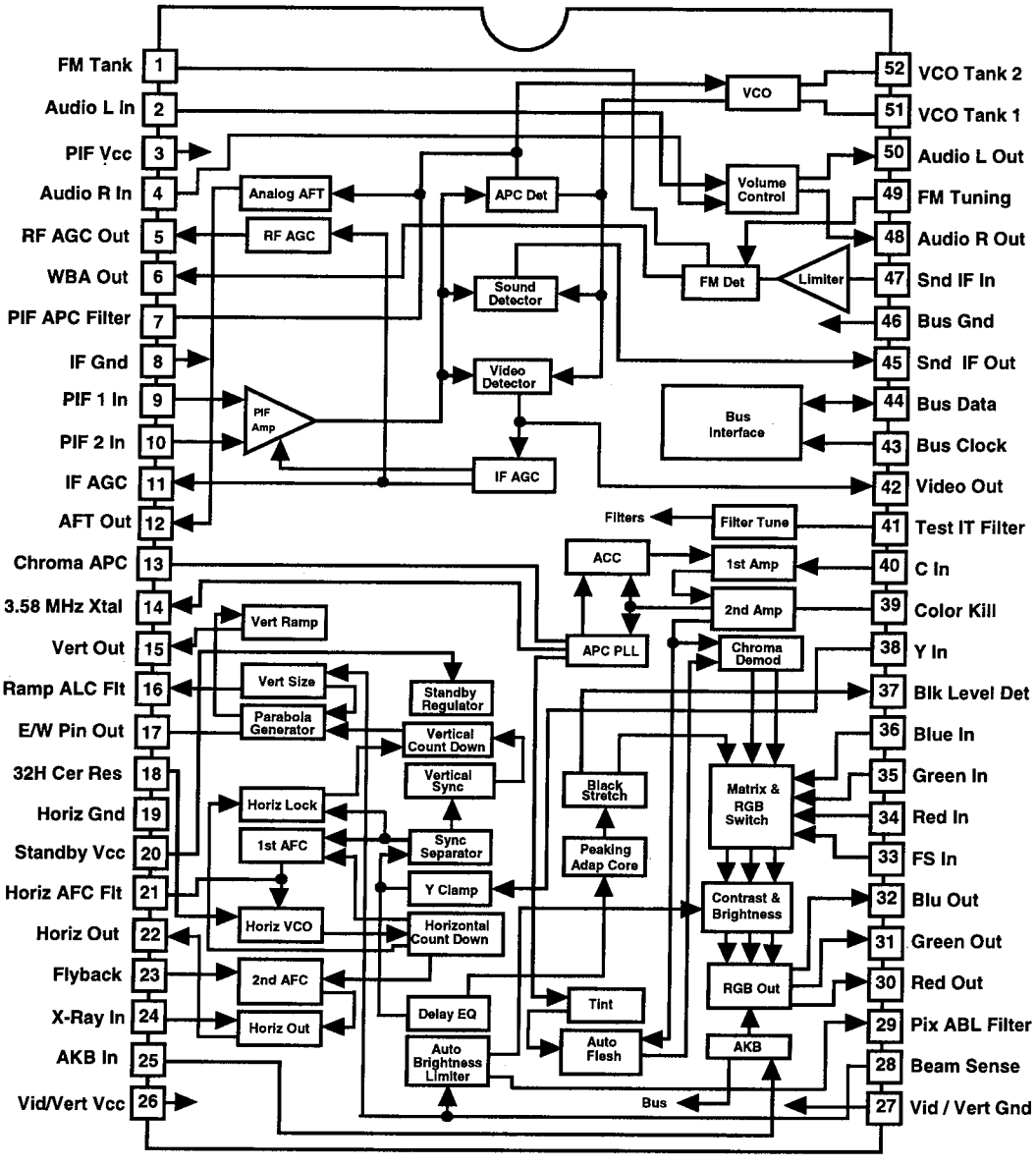


Figure 9-1, U12101, T4 IC Block Diagram

Transceiver Power Supply and Register Volatility

Each register is powered by the same Vcc as the circuit it serves. For example, the registers controlling the vertical ramp are powered by the Vid/Vert Vcc. This means that each register must be refreshed if its Vcc drops below the normal operating range. The only registers with guaranteed power-up values are Video Mute and Audio Mute.

IF Processing

The T4-Chip accepts an IF signal from the tuner circuitry and provides the processing required to strip the 45.75MHZ carrier and separate the signal into video and sound IF. There is also an AGC voltage output for signal level control. See the section on tuner operations for more information. The video is output as standard NTSC baseband video signal

Audio Detection

The sound IF signal is processed by the T4 where it is first stripped of its 4.5MHZ component. It is level limited and FM detected. It is output as a wide band audio signal.

CRT Management

XRay Protection, E-W correction and Beam Limiting are all integral circuitry within the T4. All are discussed elsewhere in this manual.

Deflection Processing

All low level vertical and horizontal deflection signal processing and control and all sync signal processing is performed within the T4-Chip. Geometry controls are available to the technician using the Service Man parameter screen or Chipper Check™ troubleshooting software. See the section on Deflection or System Control for more information.

Video Processing

The video processing circuitry in the T4-Chip receives Luma and Chroma video signals from the Video Module (F2PIP or Comb) and allows either user or technician control of the shape of the waveforms exiting to other processing circuits or the CRT. Video processing includes brightness, color, tint, contrast and sharpness. All alignments performed by the T4-Chip are controlled by the microprocessor via the I^2C bus and are available to the technician using the Service Man parameter screen or Chipper Check™ troubleshooting software. See the section on Video Processing for more information.

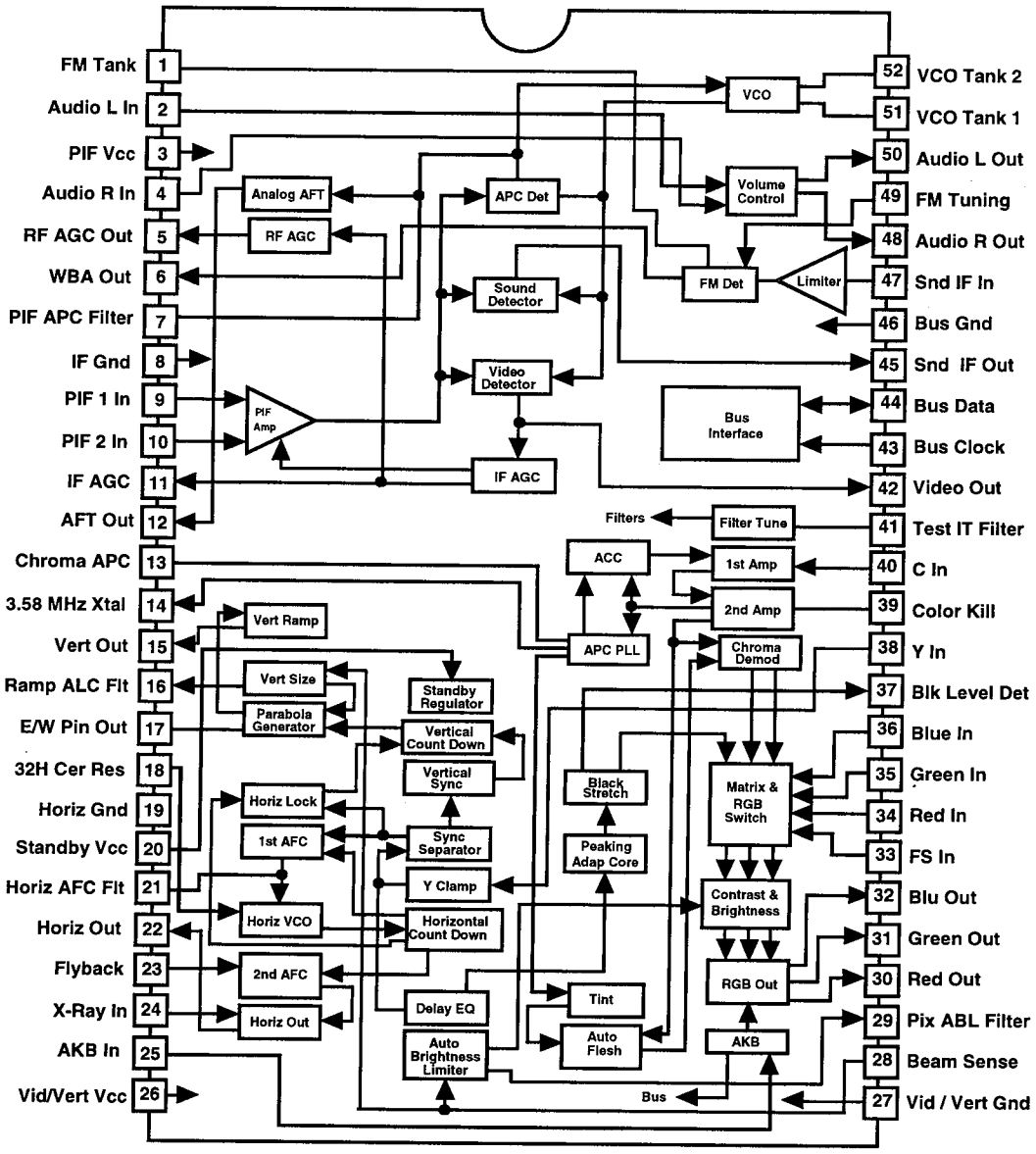


Figure 9-1, U12101, T4 IC Block Diagram (Repeated)

Analog Comb Module

The Analog Comb Module is used in place of the F2PIP Module on some models of the CTC203. Figure 10-1 is a Block Diagram of the module. Input jacks, Aux. Video/Audio and S-Video, are mounted on the module. The module expects a 1Vp-p composite video signal with negative sync.

The module has four main sections.

1. **Composite Video Switch:** The module is capable of switching between the Composite TV Video from the tuner and the Auxiliary Video Composite Video.
2. **Analog Comb Filter:** The module provides combing of the selected composite video signal and outputs combed luma and chroma.
3. **S-Video Switch:** The module is capable of switching between the combed Y/C signal and the S-Video Y/C signal which does not normally need combed.
4. **Input/Output Jacks:** The module can have 0, 3, or 5 jacks for audio and video signals.

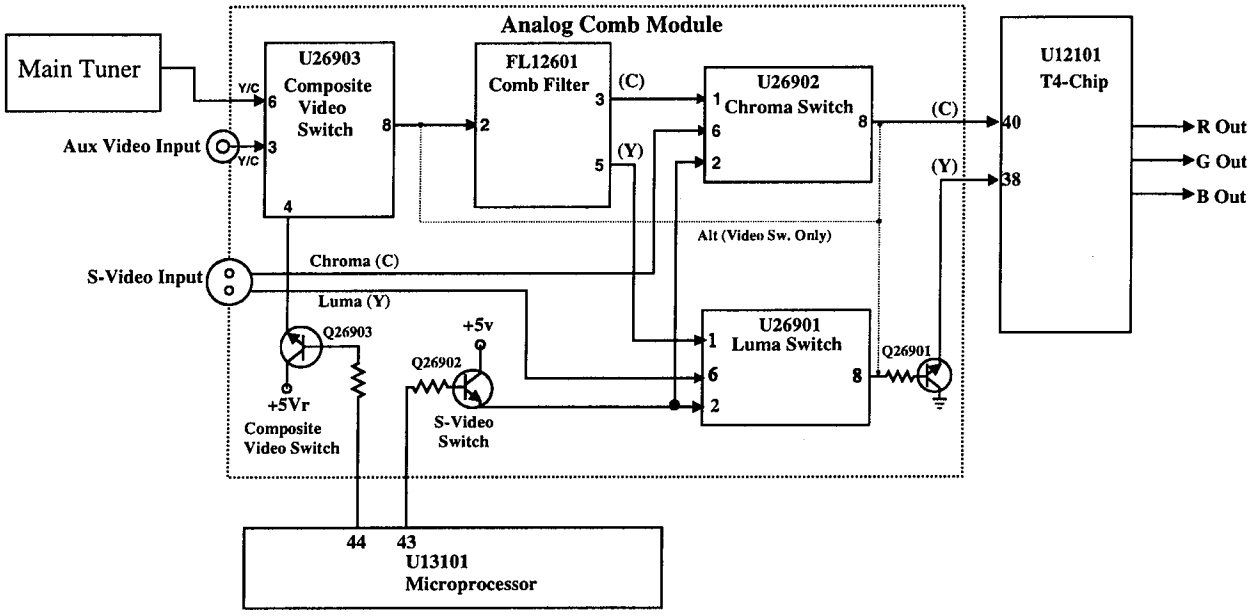


Figure 10-1, Block Diagram Analog Comb Module

The module may also be used as a video switch without using the comb filter. In such cases the comb filter, S-Video jack and S-Video switches are not loaded on the circuit board and the output of the composite video switch is applied to both the Y and C module outputs.

Composite Video Switch

Composite Video switching is handled by U26903. The IC has 2 composite video inputs; main TV Video from the tuner into pin 6, and composite video from the Auxiliary Video input jack into pin 3. Switching is accomplished using a logic line from the system control, U13101-44, to U26903-4 through composite video switch, Q26903. Main TV composite video is selected when Q26903 is OFF and the control pin is pulled LOW (~0V). When the control pin is driven HIGH (~5V) by Q26903, Auxiliary Video input is selected. The selected signal is output on pin 8.

Source	Destination	Input	Output	U26903-4
Tuner	Main	6	8	Low
Input 1	Composite	3	8	High

Figure 10-2, Composite Video Switch Control Logic

Analog Comb

The output of the Composite Video switch, U26903-8 is input to the Comb Filter, FL12601-2. A composite video color image (Y/C) is made up of color (Chroma) information that is interleaved with the black and white (Luma) signal. Chroma (C) can cause noise in the Luma (Y) portion of the video. This can appear as color noise or dot interference.

The line comb processor circuit is a combination integrated circuit and glass delay line. Its purpose is to comb (separate) a composite NTSC video signal into its luminance (B&W) component from the chrominance (color) component. Using the delay line, adjacent TV lines can be added or subtracted allowing luminance (Y) to be separated from the chrominance (C).

The luminance is output to the Luma Switch, U26901-1. The chrominance is output to the Chroma Switch, U26902-1. U26901 and U26902 are identical video switches.

Source	Selected Input	Output	U26901-2	U26902-2
S-Video Y In	U26901-6	U26901-8	Low	Low
S-Video C In	U26902-6	U26902-8	Low	Low
Main Y	U26901-1	U26901-8	High	High
Main C	U26902-1	U26902-8	High	High

Figure 10-3, S-Video Switch Control Logic

S-Video Switch

With both inputs now in S-Video format, selecting between main Y/C and S-video Y/C is accomplished using the separate video switches U26901 and U26902 located on the module. Combed Luma from the main composite video switch U26903 is applied to U26901-1 and Chroma is input to U26902-1. Luma (Y) from the external S-Video input is applied to the luma switch U26901-6. Chroma from the external S-Video input is applied to the chroma switch, U26902-6. Switching logic is controlled by system control, U13101-43 connected to the switches at pin 2 through S-Video switch, Q26902. On both U26901 and U26902 when the control line on pin 2 is HIGH, the input on pin 1 is selected for output to pin 8. When the control line is LOW, the input on pin 6 is selected for ouput to pin 8.

When the main Y/C is selected, system control turns on Q26902 placing a HIGH control signal (+5V) on both U26901-2 and U26902-2. This selects input 1 of both switches. U26901-1 is main Y and U26902-1 is main C.

To select S-Video Y/C, Q26902 is turned OFF pulling U26901-2 and U26902-2 LOW (0V). This selects the pin 6 inputs. S-Video Y is selected on U26901-6 and S-Video C is selected on U26902-6. The selected signals are output on pin 8.

Chroma is output from the module directly to the T4-chip, U12101-40. Luma is buffered by Q26901 then output from the module to the T4-chip, U12101-38.

Input Jacks

The types of input jacks available on the module may include:

- **Video Input:** (Aux Composite video).
- **S-Video Input:** that has separate Y and C video inputs.
- **Left/Mono and Right Audio Input:** Stereo or monaural audio input pair. (Audio signals pass through the module but are not processed by it.)

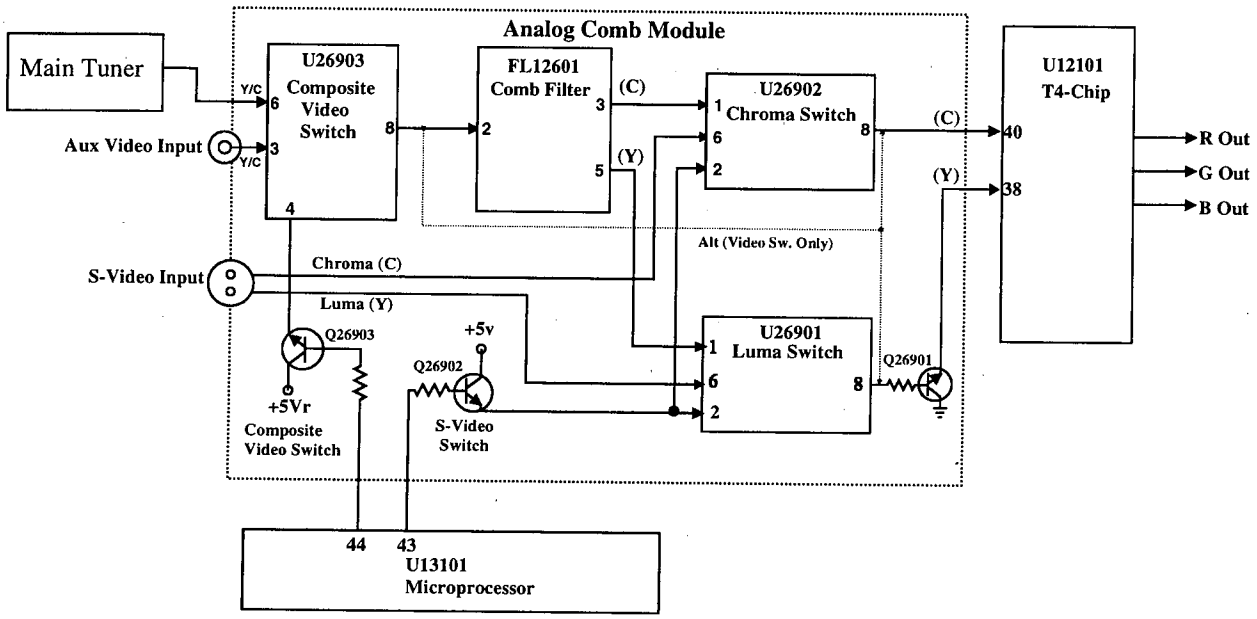


Figure 10-4, Block Diagram Analog Comb Module (Repeated)

Output Jacks

The types of output jacks that may be available on the module:

Left/Mono and Right Output: Stereo audio output pair. (These signals pass through the module and are not processed by it.)

Power Supplies

The +12V switched run supply is input to the analog comb module. The Module generates 9 and 5 Volt supplies from the supply. The Analog Comb package operates from +9V and the Video Switches operate from +5V.

Audio

Overview

Central to the CTC203 audio system is U11601, a custom audio processing IC. U11601 contains the stereo decoder, Secondary Audio Programming (SAP) decoder, audio selection switches, de-emphasis (dbx), Tone/Volume/Balance (TVB) processing, and an IIC bus interface. All functions and alignments are performed via IIC bus commands.

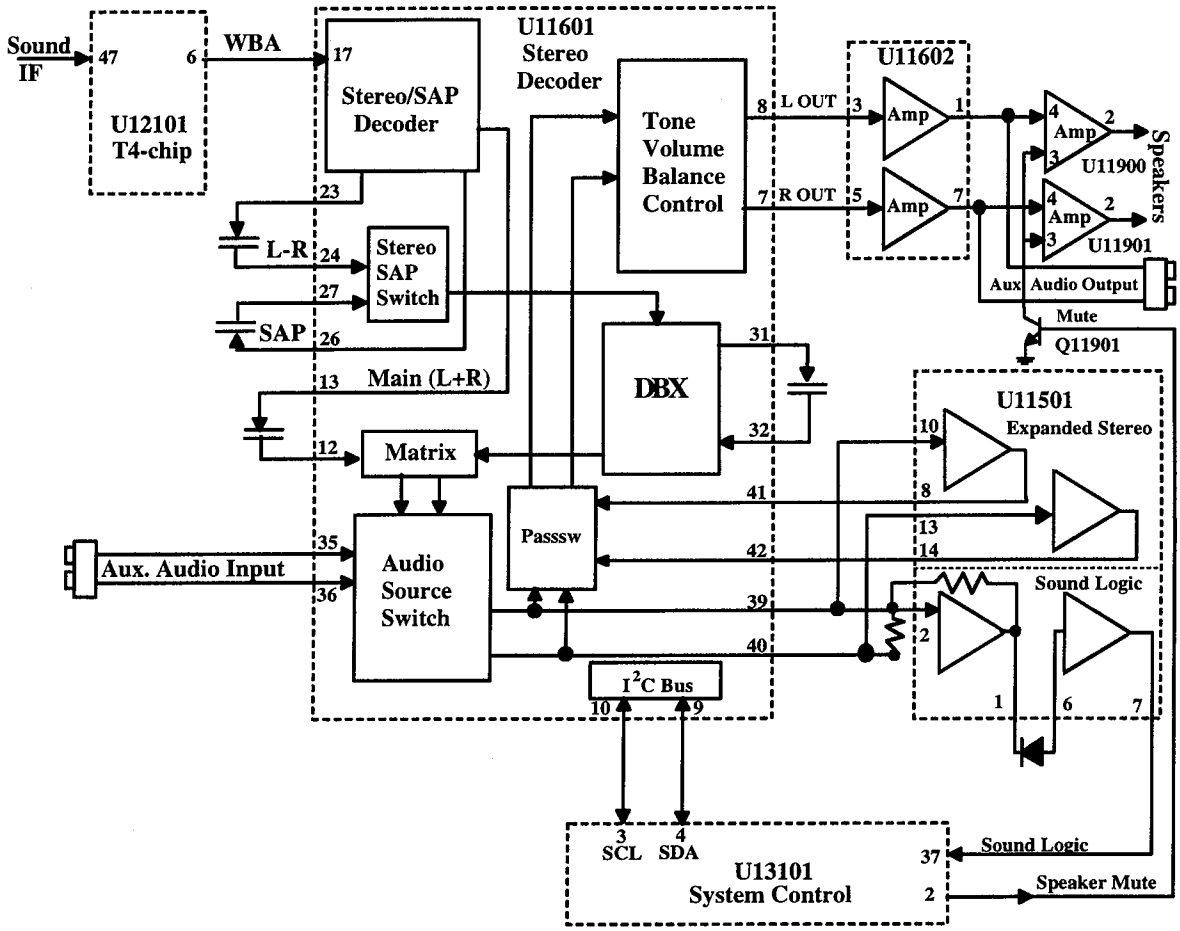


Figure 11-1, Audio Block Diagram

U11501 uses the decoded stereo output from U11601 to produce a reference DC voltage for Sound Logic and for producing the Expanded Stereo signals. U11602, a dual TL082, provides buffer amplifiers for the right and left audio output signals from U11601. The outputs of the buffered amplifiers provide signal to the Hi-Fi output jacks and power amplifiers. U11900 and U11901, both TDA7267's, are used as the power amplifiers. The output drivers can provide a 2.83Vrms signal into an 8-ohm speaker load to produce 1 Watt per channel.

Stereo/SAP Decoder

The T4-chip, U12101 decodes the sound IF and provides a demodulated WideBand Audio (WBA) output. The output of the T4 is approximately 425mVrms for a signal with a 25kHz (100%) audio carrier deviation. A resistive pad in the signal path reduces the signal to 245mV for input to U11601-17. This is the input to the Stereo/SAP decoders. The stereo and SAP decoders are Phase Locked Loops (PLL's) locking their frequencies to the stereo pilot and SAP subcarrier in the WBA. The Voltage Controlled Oscillators (VCO's) for the two decoders are aligned via the IIC bus. When a stereo pilot and/or SAP pilot are detected, a "presence" status flag is made available to the IIC bus where it can be read by the system control microprocessor.

The recovered main (L+R) signal is passed through a low pass filter (LPF) to suppress the SAP and then the pilot carrier is cancelled. After the pilot is cancelled it then passes through a second LPF to block the L-R signal. The frequency characteristics are flattened (de-emphasized) and it is then input to the matrix.

The L-R signal follows the same path as the main signal until after the pilot canceling. The L-R has no carrier signal, as it is a suppressed carrier double-sided amplitude modulated signal. The pilot canceling signal is used to regenerate the carrier signal to enable the L-R signal to be demodulated. The demodulated L-R signal is input to the Stereo/SAP switch.

SAP is an FM signal that has a carrier frequency 5 times the horizontal frequency. The SAP signal is taken from the WBA using a SAP band pass filter (BPF). The signal is then FM detected and filtered and de-emphasized. It is then input to the Stereo/SAP switch.

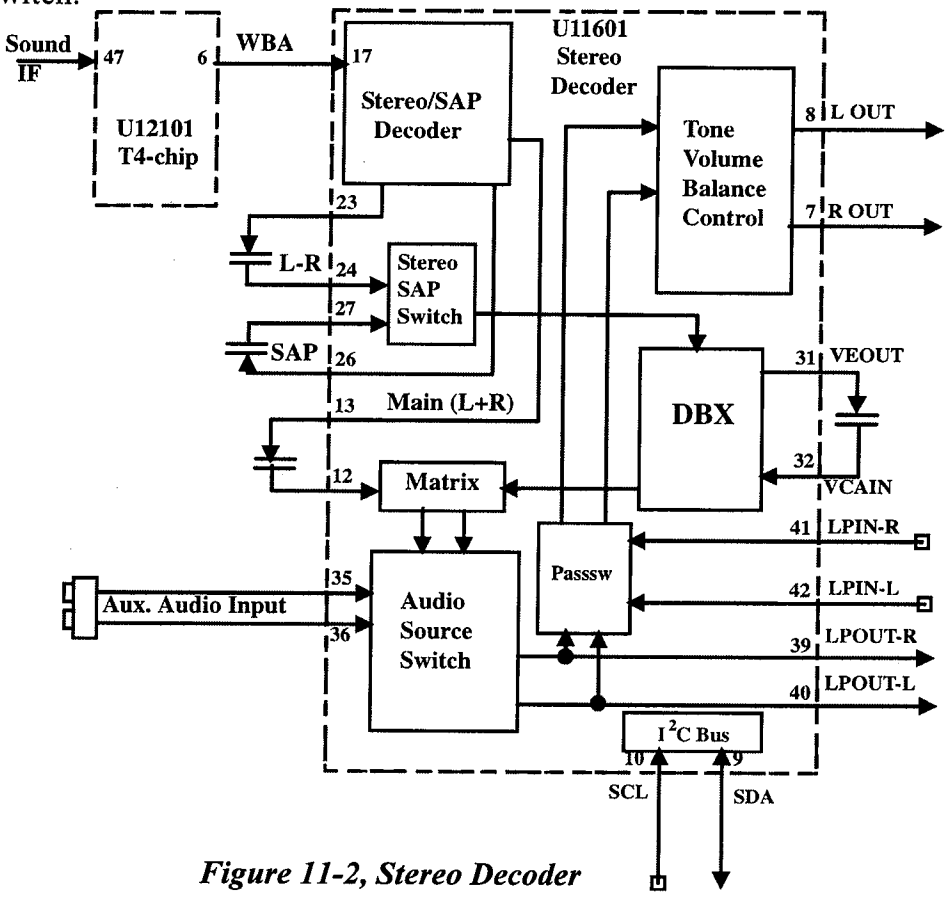


Figure 11-2, Stereo Decoder

Stereo/SAP Switch

The Stereo/SAP switch is IIC bus controlled. It selects between the L-R and SAP signal as to which is input to the DBX

DBX

Either the L-R stereo or SAP signal is sent by the Stereo/SAP switch to the dbx expander. The input signal passes through a fixed de-emphasis circuit and then through a variable de-emphasis (VE) circuit. VE OUT is passed through an external capacitor and is applied to VCA IN (voltage controlled amplifier). The VCA output is input to the matrix control. All dbx expander alignments are IIC bus-controlled.

Matrix

The matrix accepts signals L+R, L-R and SAP. The matrix turns these into stereo left, stereo right, mono and SAP signals according to IIC bus commands and whether there are stereo and SAP pilots present. The output of the matrix is input to the audio source switch.

Audio Source Switch

The audio source switch has inputs from the matrix control (ST-L, ST-R) and from the Auxiliary Audio Input Jacks. The signal output by the audio switch is controlled by the IIC bus. The output of the audio switch is input to the passsw and output on pins 39 (LPOUT-R) and 40 (LPOUT-L).

Lpout (Loop Port Out)

Pins 39 and 40 output the decoded audio signal. These signals are used in the CTC203 to produce the reference voltage for the Sound Logic control and to produce the Expanded Stereo signals. These signals are always present if the stereo decoder is working properly and should be a constant 490mVrms for a 100% modulated signal.

Lpin (Loop Port In)

Pins 41 and 42 input expanded stereo signals in the CTC203 after the Lpout signals are conditioned by an external expanded stereo circuit, ½ of U11501. These signals are always present if the stereo decoder is working properly.

PASSSW (By-Pass Switch)

The by-pass switch has inputs from the audio source switch and from Lpin, expanded stereo signal. The pass switch is IIC bus controlled and applies the selected output to the Volume/Bass/Treble control.

Tone/Volume/Balance Control

This sound processor block contains the Tone/Volume/Balance (TVB) section. The signal is processed according to the customer settings of volume, bass, treble, and balance. The controlled signal emerges at output pins 34 and 35. Zero-dB level is 500mVrms.

IIC Bus

The IIC bus is internal to U11601 and provides the logic for controlling the Stereo/ SAP switch, Audio Source switch and the Passsw switch. In addition all alignments for the IC are performed electronically over the bus.

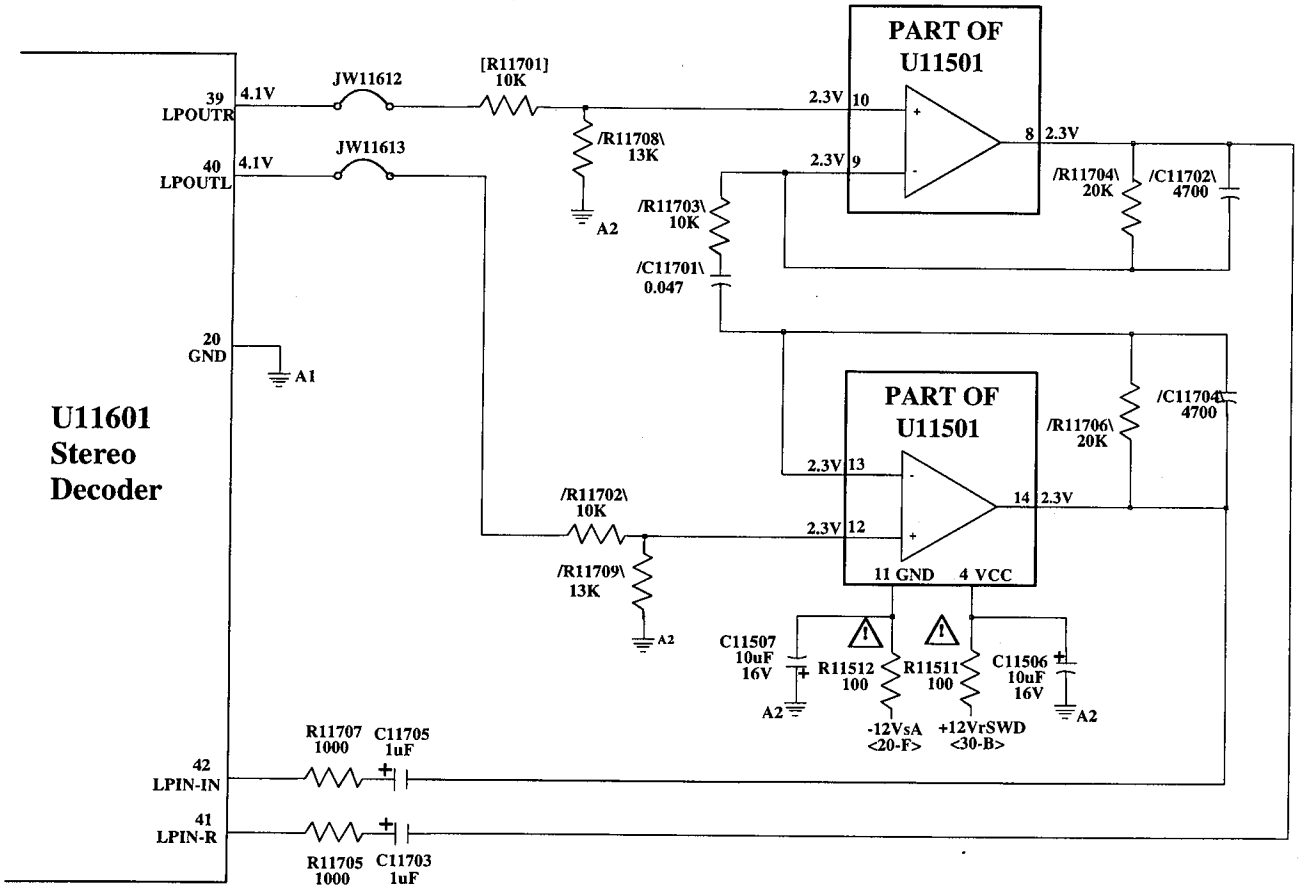


Figure 11-3, Expanded Stereo

Expanded Stereo

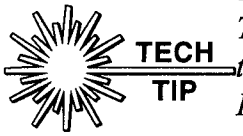
Half of U11501 and its associated parts make up the Expanded Stereo circuit (see Figure 11-3). Decoded Audio signals are output at U11601 pins 39&40, LPOUTR&LPOUTL. The signal should be a constant level 490mVrms with 100% audio input signal. The signals are input to the two U11501 operational amplifiers. The outputs of the two U11501 amplifiers mix the left and right channel information through R11703 and C11701. The Expanded Stereo hardware widens the sound field to produce a perceived increase in stereo separation so that sound effects and music seem to envelop the listener from many directions. The output of the Expanded Stereo is input back to U11601 pins 41&42, LPIN-R & LPIN-L, and into the by-pass switch.

Expanded Stereo is a user selectable option in the Audio Menu. The by-pass switch is IIC bus controlled by the settings in the Audio menu. When the user selects Expanded Stereo in the Audio menu, then the Passsw outputs the Expanded Stereo signals to the TVB control. The Expanded Logic circuitry is always active.

Sound Logic

Sound Logic is a user selectable option in the Audio menu. The Sound Logic circuit reduces the annoying blasts in volume during commercial breaks, and also amplifies softer sounds in program material. Its purpose is to eliminate the need for the user to constantly adjust the volume.

The Sound Logic circuit is shown in Figure 11-4. The sound Logic system is quite simple. The only hardware involved is an audio level detector circuit made from half of U11501 and associated parts. The circuit integrates the level of the audio versus time and outputs a DC voltage. The detected DC level is read by system control U13101-37. System control then adjusts the volume based on an internal algorithm. The Sound Logic detector is always active but is ignored by the microprocessor when Sound logic has not been activated by the user.



To test the detector, connect a DVM to the sound logic output (cathode of CR11503). Tune to a channel with strong audio, preferably mono, or provide a 1kHz sine wave to the Auxiliary 1/Mono Audio input jack. The signal level at U11601 pins 39&40, LPOUTR & LPOUTL, should be a constant level 490mVrms with 100% audio signal. The detector output should be approximately 4VDC. Tune to a channel without audio or remove the signal input to the Aux 1 input jack. The detector output should be less than 100mVDC.

The detector output should vary with the audio signal level. This can be verified by tuning to a channel with programming or providing a program input to the Aux 1 input and observing that DC voltage varies with sound level.

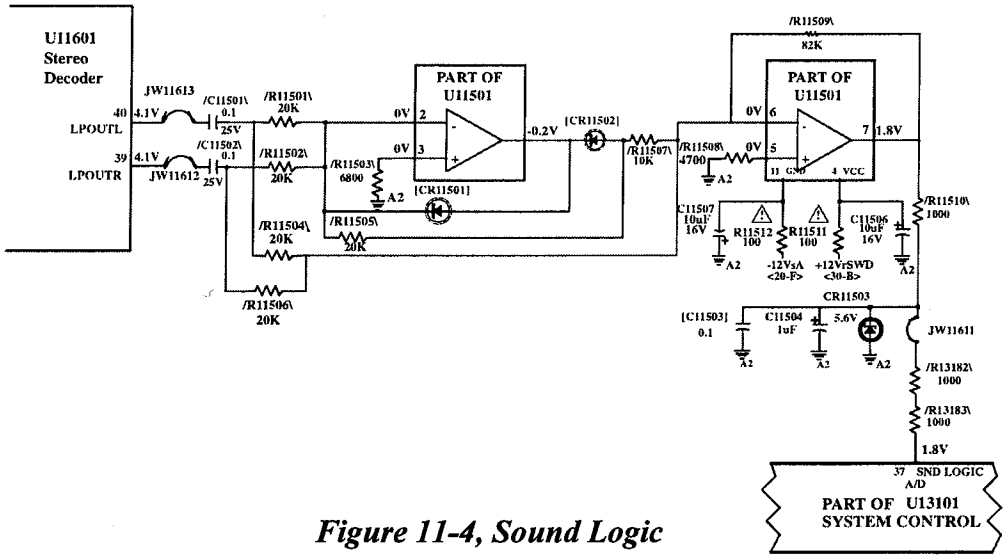


Figure 11-4, Sound Logic

Audio Buffers

Audio buffers (Figure 11-5) are used to isolate U11601 from the HI-FI jacks and to drive the power amplifier stage. U11602 is used as the audio buffer and HI-FI jack driver. It utilizes an inverting, one-stage amplifier with a gain of approximately 7. It isolates the Stereo Decoder from various load impedances applied to the HI-FI jacks and provides about 1.75V at the jacks at full power.

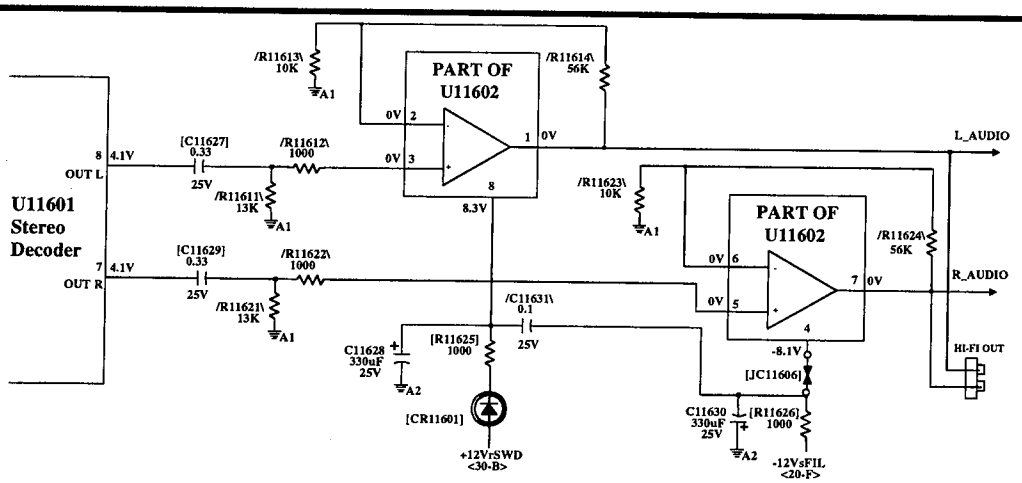


Figure 11-5, Audio Buffers

Power Amplifiers

There are two power amplifiers, U11900 & U11901. They can produce up to 1W per channel into an 8 ohm speaker. CTC203 speaker impedance is 8 ohms. No external speaker connection is provided.

To prevent transients in the speakers when the instrument is turned on or off and allow the customer to manually mute the speakers, the power amplifiers may be muted. When pin 3 of the amplifier modules is high (~8V), the amplifier operates normally. When pin 3 falls to less than +1V, the output is muted. A mute signal from system control, U13101-2 to the mute switch, Q11901 controls pin 3. U13101-2 is an open collector output. During normal operation the output is on placing a low on the pin. With no bias on the Mute Switch, Q11901-B, it is off. This leaves U11900-3 & U11901-3 open and the amplifiers run normally.

During mute, the open collector output from system control, U13101-2 is open. Q11901 bias is now provided by the voltage divider of R11917 & R11918 placing about +5V on its base. The mute switch turns on, placing a low voltage on U11900-3 & U11901-3, muting the amplifiers.

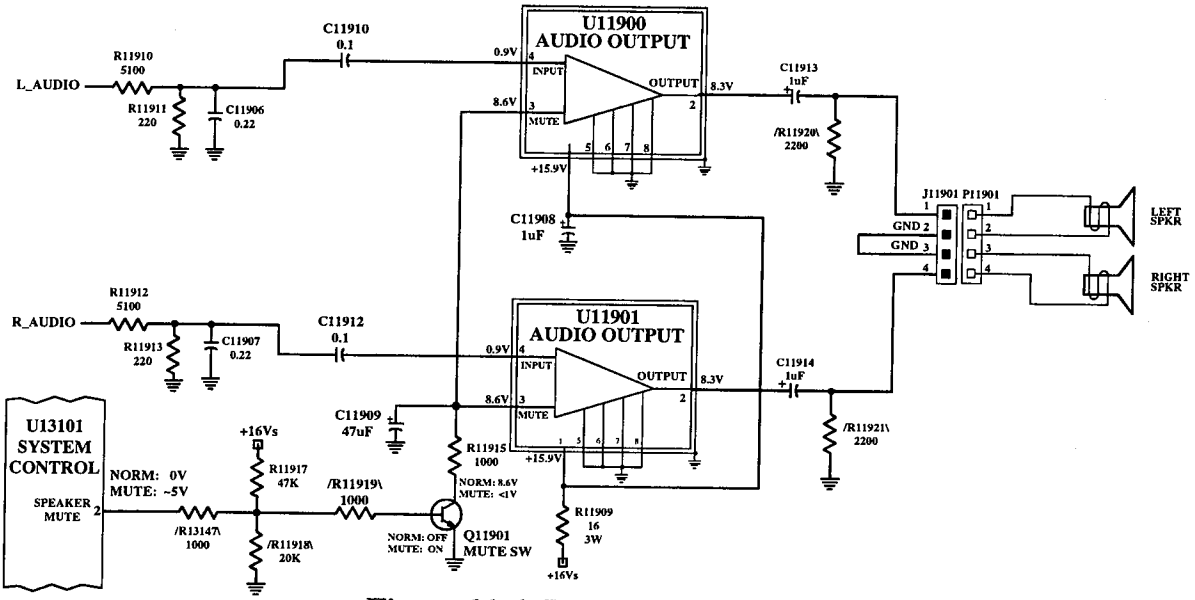


Figure 11-6, Power Amplifiers

GEMSTAR

Overview

TV Guide Plus+ is an interactive on-screen program guide generated by the GEMSTAR module that lists TV schedules for an area and allows the TV to have direct control of a cable box and VCR. The program information is carried during the Vertical Blanking Interval (VBI) on lines 10-20 on selected network channels. The GEMSTAR module contains memory to store the TV Guide Plus+ data, OSD control and outputs for GEMSTAR specific displays, the user interface for GEMSTAR and universal remote control codes (needed along with the IR Mouse to allow for one-touch recording from the TV guide). The GEMSTAR guide uses the PIP (on chassis models with the PIP feature) to view the selected channel while in the guide. Figure 12-1 below is a block diagram of the GEMSTAR module.

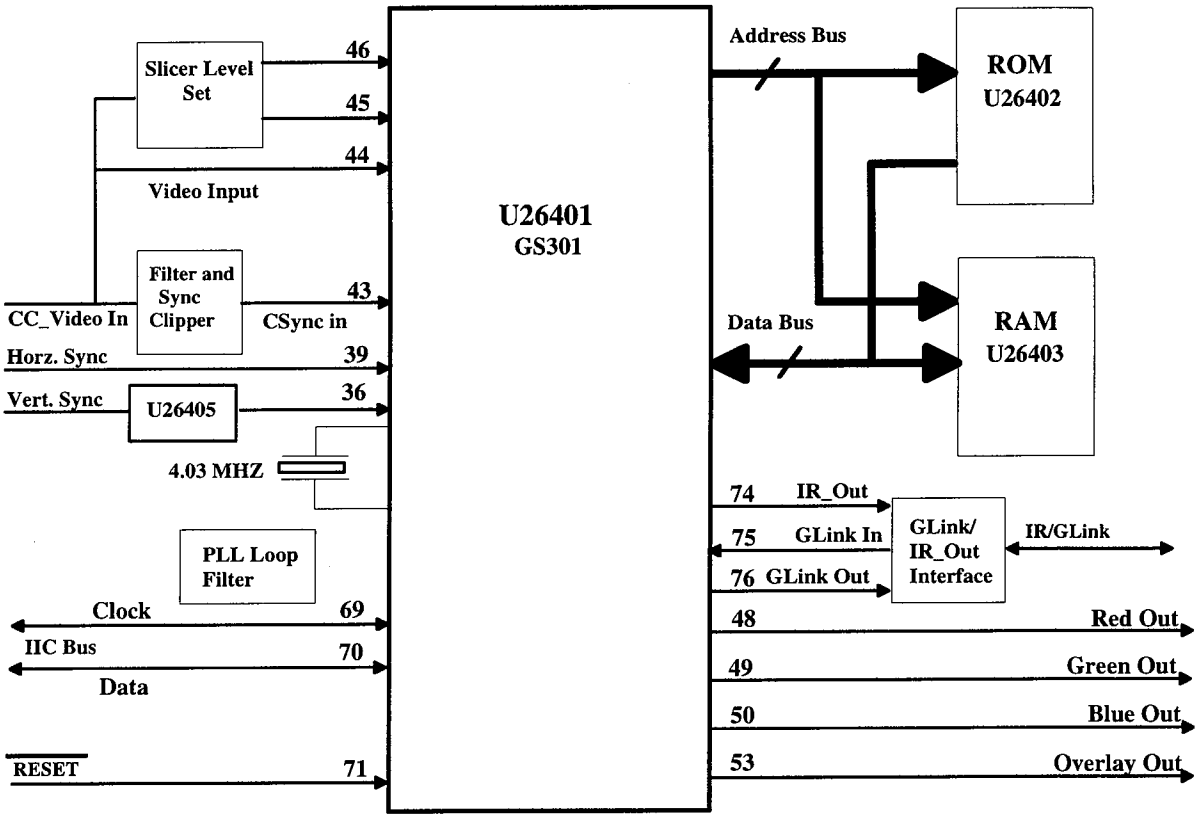


Figure 12-1, GEMSTAR Block Diagram

The minimum guaranteed RF signal level for uninterrupted operation is 100uV @ 75 ohms. The GEMSTAR OSD is summed with the main micro OSD and input to the RGB inputs of the T4-chip. The OSD for GEMSTAR is intended to have no alignment. There are EEPROM locations that control the GEMSTAR OSD position available through the service menu if needed. The centering of the PIP in the Guide may require alignment after servicing. A service command is provided to allow the PIP position to be aligned.

U26401 PIN OUT

Port Type Definition

I – INPUT

O – OUTPUT

I/O – BIDIRECTIONAL

P - POWER

PIN	PIN Name	Type
1	CAS	O
2	A0	O
3	A1	O
4	A2	O
5	A3	O
6	A4	O
7	A5	O
8	A6	O
9	A7	O
10	A8	O
11	A9	O
12	VDD0	P
13	VSS0	P
14	A10	O
15	A11	O
16	A12	O
17	A13	O
18	A14	O
19	A15	O
20	A16	O
21	A17	O
22	CSO	O
23	D7	I/O
24	VDD1	P
25	D6	I/O
26	D5	I/O
27	D4	I/O
28	D3	I/O
29	D2	I/O
30	D1	I/O
31	VDD2	P
32	VSS1	P
33	D0	I/O
34	OVL IN	I
35	CSI	O
36	VERT	I/O
37	DRAM OE	I/O
38	PDOWN	I/O
39	HSYNC_IN	I
40	VSS2	P

PIN	PIN Name	Type
41	AVSS1	P
42	AVDD2	P
43	V/SYNC_IN	I
44	VIDEO IN	I
45	VIDEO H IN	I
46	VIDEO L IN	I
47	TH CAP	O
48	R OUT	O
49	G OUT	O
50	B OUT	O
51	AVDD0	P
52	AVSS0	P
53	OVL OUT	O
54	TEST1	I
55	B IN	I
56	G IN	I
57	B IN	I
58	VVREF CAP	O
59	VVREF	I
60	AVSS1	P
61	AVDD1	P
62	PO	O
63	VCNT	I
64	R VCO	I
65	VDD3	P
66	OSCI	I
67	OSCO	O
68	VSS3	P
69	I2C CLOCK SCL	I/O
70	I2C DATA SDA	I/O
71	RESET	I
72	TEST0	I
73	VDD4	P
74	IR OUT	O
75	GLINK IN	I
76	GLINK OUT	O
77	RAS	O
78	MWE	O
79	CASO	O
80	VSS4	P

Pin Desciptions:

VDD	Digital Power Pin
VSS	Digital Ground Return
AVDD	Analog Power Pin
AVSS	Analog Ground Return
A0-A17	Address Bus to RAM and ROM
D0-D7	Bi-directional Data Bus
RAS	DRAM Row Address Strobe
CAS0-1	DRAM Column Address Strobe
MWE	Memory Write Enable
CS0-1	ROM Chip Selects
DRAM OE	Output Enable Control for Dram, External Pull-up
SCL, SDA IIC	Interface, Bi-directional serial Clock and Data
IR Out	IR Out goes low when the LED in the IR Blaster is to be turned ON
R Out	Red Output used to produce the overlay for the current TV picture
G Out	Green Output used to produce the overlay for the current TV Picture
B Out	Blue Output used to produce the overlay for the current TV picture
OVL Out	Overlay Output, Goes High when there are signals on R,G, B OUT
VVREF	Voltage reference input set by external voltage devider
VVREF Cap	Voltage reference filter cap
VIDEO IN	Composite Video input to VBI data slicing comparator
VIDEO L IN	VBI slicer level switch for setting level on TH Cap
VIDEO H IN	VBI slicer level switch for setting level on TH Cap
TH Cap	Storage capacitor
HSYNC IN	Horizontal sync Input for use in generating OSD graphics
VERT	Vertical Sync Input for use in generating OSD graphics
V/SNYC IN	Composite Sync Input. Composite Sync is taken from the composite video signal used in VBI data slicing.
OSCI	Crystal Oscillator Input
OSCO	Crystal Oscillator Output
PO	Charge pump output of the phase/frequency comparator fed to the loop filter.
VCNT	Input from the loop filter
R VCO	Pull-up resistor for the voltage controlled oscillator (VCO) control.
RESET	Power On Reset (POR) input. Negative going pulse forces U26401 to return to its initialized state.
TEST0,1	IC fabrication tests.

Controller

U26401 is an ASIC (Application-Specific Integrated Circuit) designed specifically for the GEMSTAR module. It has the following features.

- Custom microprocessor with on-chip Read Only Memory (ROM).
- Memory Controller for Dynamic Random Access Memory (DRAM) and ROM
- Direct Memory Access (DMA) controller for the video overlay.
- Sync Separator.
- RGB D/A outputs.
- Vertical Blanking Interval (VBI) data slicer and acquisition module.
- IIC communications module.
- Power Fail Shutdown mode.

Operation

TV Guide Plus+ program information is transmitted during the VBI on lines 10-20 on selected network channels similar to closed captioning transmissions. Figure 12-2 below is a Block Diagram of the Video signal path in a CTC203.

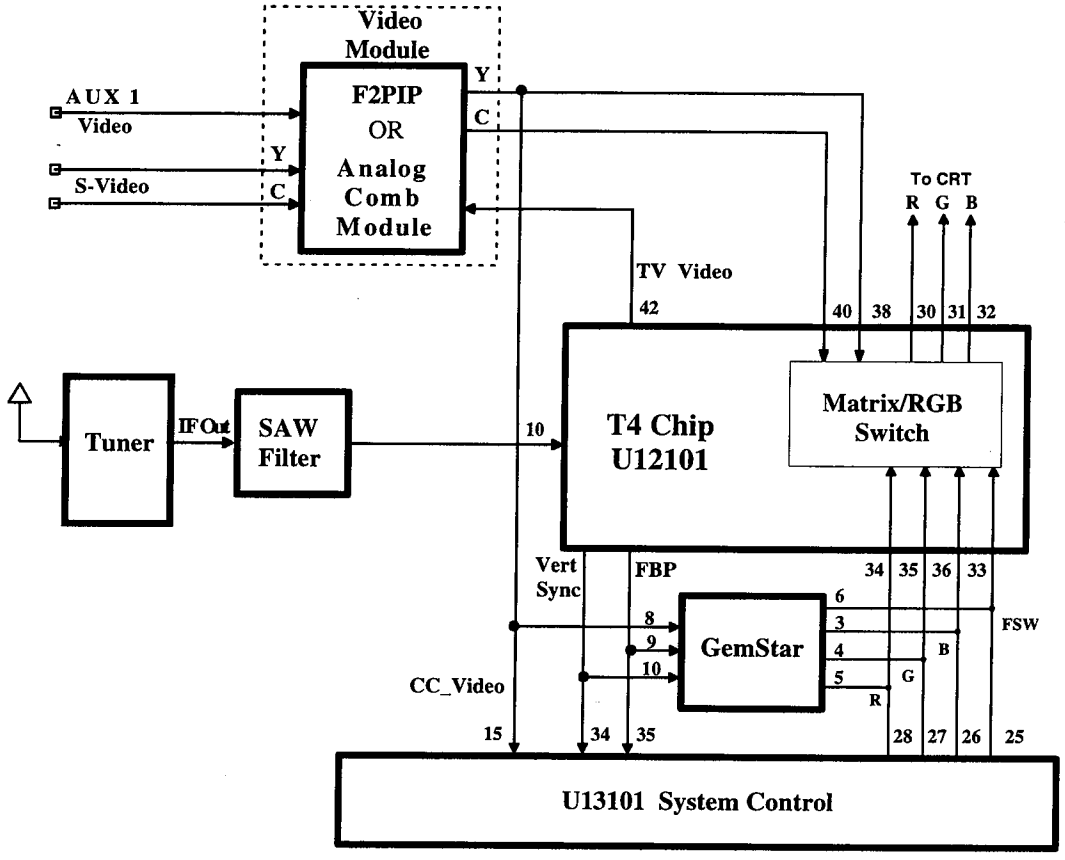


Figure 12-2, CTC203 Video Signal Path

CC_Video is taken from the luminance line (Y) after the Video Module (F2PIP, Analog Comb) and before the T4-chip, U12101. It is input to the GEMSTAR module along with Vertical Sync and Horizontal Flyback Pulse to decode the program information.

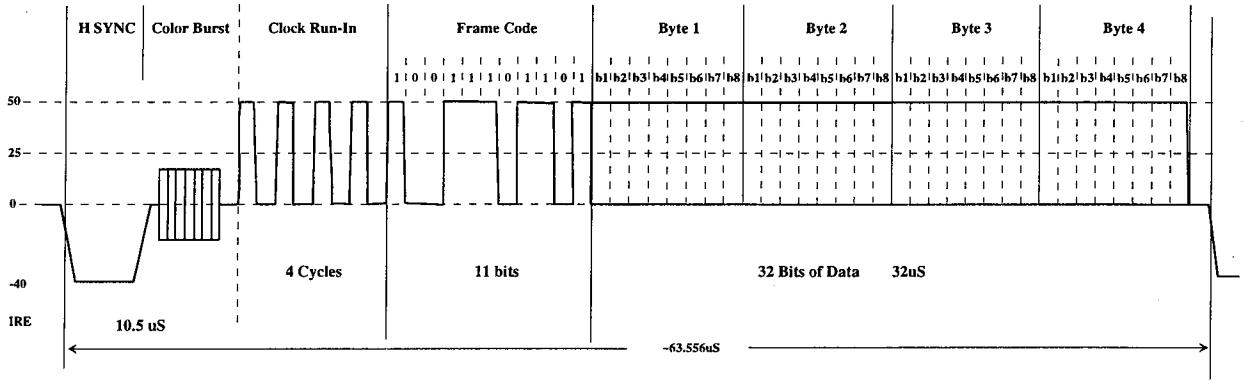


Figure 12-3, Video Signal with GEMSTAR Data

Figure 12-3 is a representation of a horizontal scan line with GEMSTAR data encoded in the video signal. The waveform is similar to line 21 used for Closed Captioning data (see System Control). The transmission consists of 4 cycles of a Clock Run-In, 11 bits for a Frame Code and 4 bytes of data. A byte of data is made up of 8 bits. The midpoint of the clock (half amplitude or 25 IRE) should be the same as the midpoint for the frame code and data bits.

CC Video

GEMSTAR data is detected using a data slicer internal to ASIC U26401. GEMSTAR data is synchronized to the ASIC by a sequence of 4 clock cycles (Run-In Clock) of 503KHz after the horizontal sync and color burst. The Run-in Clock is in phase and has the same amplitude as the following data. This is followed by an 11 bit Frame Code that describes what type of data is being transmitted. Each line contains 4 bytes of data. Each byte of data is made up of 8 bits for a total of 32 bits of data.

Pins 45,46, Video L In and Video H In, are VBI data slicer level switches used to set the slicing level. The slicing level is set on Pin 47, TH CAP, which holds the slicing level for the duration of the scan line being decoded.

Sync

There are 3 sync inputs to the ASIC; Horizontal, Vertical and Composite.

Horizontal sync is applied to the GEMSTAR module on pin 39. The horizontal from the fly back pulse is filtered and clipped and then applied to the ASIC. Horizontal sync is used along with composite sync for synchronization of the VBI data slicer. It is also used for generating the Guide OSD output so that it is synchronized with the incoming video signal.

Vertical sync is applied to the GEMSTAR module on pin 36. Vertical from deflection is used to trigger a mono-stable multivibrator, U26405, which outputs the desired square wave for the ASIC. Vertical sync is used along with composite sync for synchronizing of the VBI data slicer.

CC_Video In is also fed to the Filter and Sync Clipper circuit to extract composite sync. Composite sync is applied to V/Sync In, pin 43. The composite sync is used along with vertical and horizontal sync by the VBI data slicer for timing information. It is used to extract the GEMSTAR data when the regular sync is not available. This allows the GEMSTAR module to acquire data even when the set is "OFF" (see Power below).

If the GEMSTAR module does not have sync present then there will be no Guide output. If the sync is present but unstable then there may be a torn Guide OSD output.

Power

The GEMSTAR module needs to be able to collect Guide Data while the set is "OFF". This requires that the instrument's power supplies be "ON" while data is acquired. Instead of complicating the power supply design to allow part of the chassis to be "ON" to collect this data, the instrument turns "ON" all of the chassis power supplies with the exception of supplies generated by the Flyback. This mode is active after the user has gone through the setup routine to search for channels, after a power dropout to collect time of day and during normal scheduled times set up by GEMSTAR,.

Normal scheduled download times are always "Local Time" and occur at the following times: 2:05AM, 7:00AM, 10:45AM and 2:00PM. Normal scheduled download times are administered by local area broadcasters and cable companies.

Reset

Pin 71 is used for Power On Reset (POR). The pin is a Schmitt trigger input that is forced low to reset the ASIC. When reset the ASIC will return to its initialized state. POR is also used to take the ASIC out of its low power save state. The ASIC enters this low power state if the +5.2 volt supply is detected going down.

IIC Bus

The system control, U13101, communicates with the GEMSTAR ASIC via the GEMSTAR I^2C bus. The Data and Clock lines are input to pins 70 and 69. U13101 auto-detects the GEMSTAR module by polling the module over the I^2C bus lines. If the module is not detected there will not be a menu item for "GUIDE PLUS+ Menu" in the Main instrument Menu.

RGB Output

Pins 48, 49 and 50 are the Red, Green and Blue outputs. These 3 pins along with pin 53, overlay out, are used to output the OSD to the T4, U12101. The RGB outputs range from 0V (no color) to approximately 0.92 V (full intensity color).

PIN 53, overlay out, is a TTL compatible signal that is >1.5V any time there is an active output on the RGB pins.

Memory

The GEMSTAR module has two types of memory, Dynamic Random Access Memory (DRAM) and Read Only Memory (ROM).

The GEMSTAR module uses DRAM memory to store Guide Plus+ data. If 5V is removed from the module for an extended period the Guide Plus+ data will be lost.

The GEMSTAR module uses ROM memory to store the Guide Plus+ Menus, Universal IR codes and ASIC programming information.

The ASIC uses 18 Address lines and 8 Data lines to communicate with the DRAM and ROM. There will be communication pulses on these lines whenever the Guide Plus+ menu is accessed.

IR Blaster

Pin 74 is the IR output from the ASIC. It allows the GEMSTAR to control a cable box if the IR Blaster is connected to the cable box and the module was properly setup. When the GEMSTAR is setup to control a cable box, the instrument's tuner is locked to the input channel or video input used by the cable box. The GEMSTAR module will change the channel number OSD even though the tuner channel is not changed.

The IR Blaster also allows for "One Touch Recording" if the blaster is connected to your VCR.

Diagnostic Test

The GEMSTAR module has an internal Diagnostic Test that can be accessed with the remote control for Guide Plus+. NOTE: Accessing the Diagnostic Test will erase all Guide Plus+ data from memory.

Tune the instrument to a channel with known good Guide Plus+ VBI data.

- Select "Main Menu"
- Select "GUIDE PLUS+ Menu"
- Select "GUIDE PLUS+ Setup"
- On the remote control press "Go Back"
- On the remote control press "TV'

This will bring up the GEMSTAR Diagnostic Test. The GEMSTAR will perform 6 module tests.

1. ROM. The module will test the on board ROM to see whether information is being correctly read.
2. RAM. The module will test the on board RAM to see whether information is being correctly written and read.
3. VBI. The module will determine whether VBI data is being received. If this test fails make sure the set is tuned to a channel with known good VBI data.
4. GLINK. This test is used only in the factory and will always show "Failed".
5. IR. This IR test is performed in the Factory through the GLINK and will always Fail for the servicer. To test the IR Link, attach the IR cable and place the LED in front of a VCR and attempt a One Touch Recording. See the Owners manual for specific information on how to set the unit up for One Touch Recording.

6. VBI Packet Statistics: This test is a VBI download test. The number of VBI data packets received and decoded for the current data channel are shown as either "good", "fixed" or "bad". The majority of the packets should be shown as "good". The number of "bad" packets is a product of how well the ASIC is able to decode the incoming data. "Bad" data can be caused by a weak video input signal. If there is a strong video signal available then the GEMSTAR module should be checked.

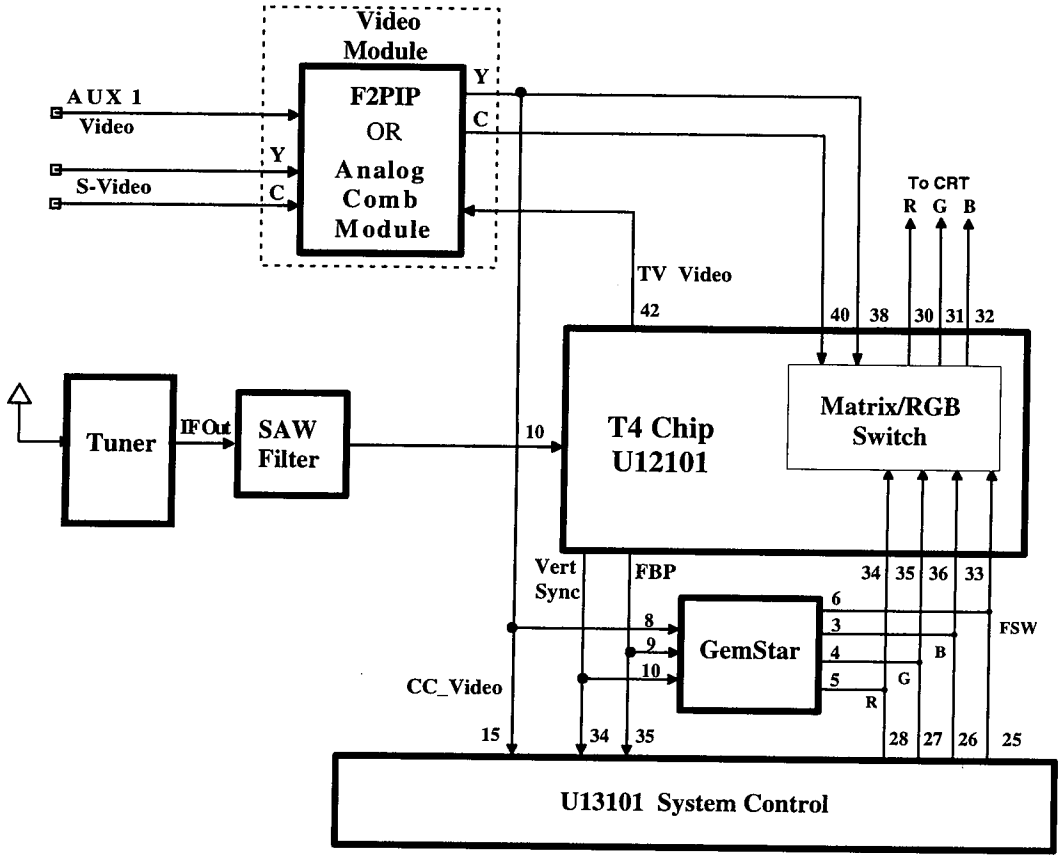


Figure 12-2, CTC203 Video Signal Path (Repeated)

Troubleshooting

No Guide Plus+ Menu Item in Main Menu.

- Check to see if the main menu on the instrument includes the item "GUIDE PLUS+ Menu". If the menu item is not present U13101 is unable to communicate with the GEMSTAR module.
- Check the cable(s) to the GEMSTAR module. Make certain all connectors are seated properly. If this is the problem the menu item will appear once the connectors are seated properly.
- Check for +5.2 volts on the GEMSTAR module and to the VCC pins of the ICs.
- Check the 4.03MHz oscillator is running and at the proper frequency on the ASIC.
- Check to see if there are pulses present on the IIC bus data and clock lines.

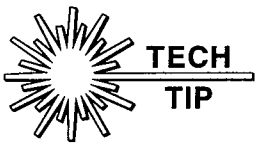
Guide Plus+ Menu Item in Main Menu present but No Guide Plus+ Menu

These signals may be checked on the connector, J26402.

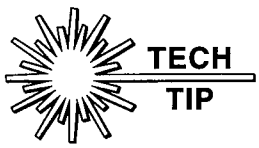
- Check for Vertical and Horizontal sync pulses on pins 6 (GEM VERT) and 7 (GEM FBP1).
- Check for Composite Video at pin 8.
- Check Reset on pin 6 (GEM RESET). It should be about +5.2V.
- Check for RGB output at pins 11, 12 and 13.
- Check for Overlay Out at pin 10 (FSW).
- Recheck all cable(s) and insure they are seated properly.

Incorrect or No Data Stored for Guide.

- Check that instrument is tuned to a strong channel with GEMSTAR VBI data.
- Use diagnostic test to check module operation.
- Check owners manual on Guide Plus+ setup procedures.



The CTC203 Electronic Service Data contains a complete schematic of the Gemstar module. If the technician wishes to troubleshoot further into the module, begin by following the above signals to their ends or beginnings. There are various components in these signal paths whose failure can cause improper module operation.



The Guide Plus+ software has a special learning/demo mode available to the consumer. Most sets contain a pin inserted into the VCR CONTROL jack on the rear panel of the set automatically enabling this mode. The pin activates the mode every time the set is turned on. Although the set immediately enters the demo mode it can be taken out via on-screen menu selection. However, as long as the pin is the rear panel jack, the set will not receive channels above VHF 13 whether the demo mode is active or inactive. The set must be turned off, the pin removed and the set turned back on for normal operation to return.

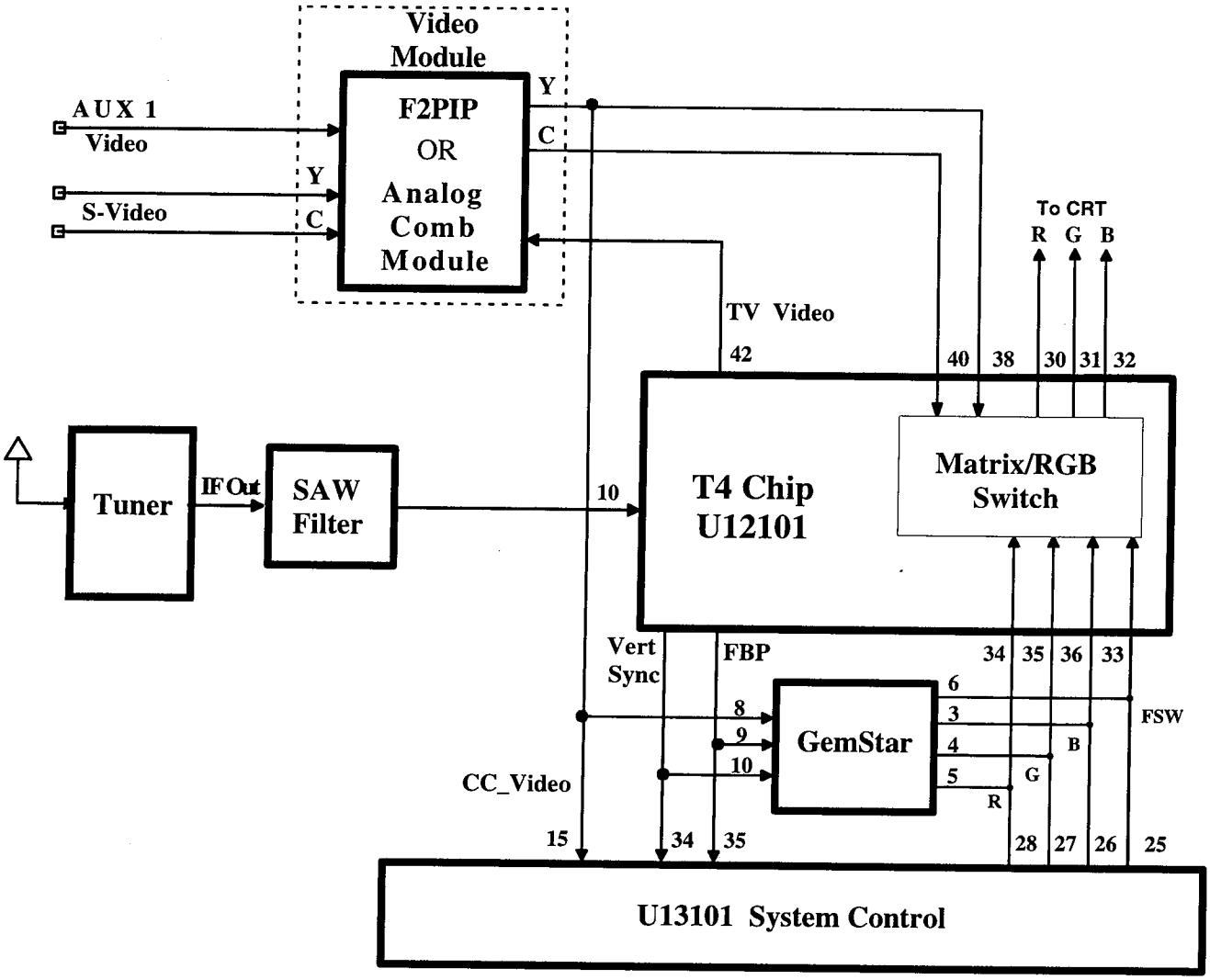
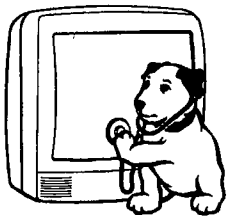


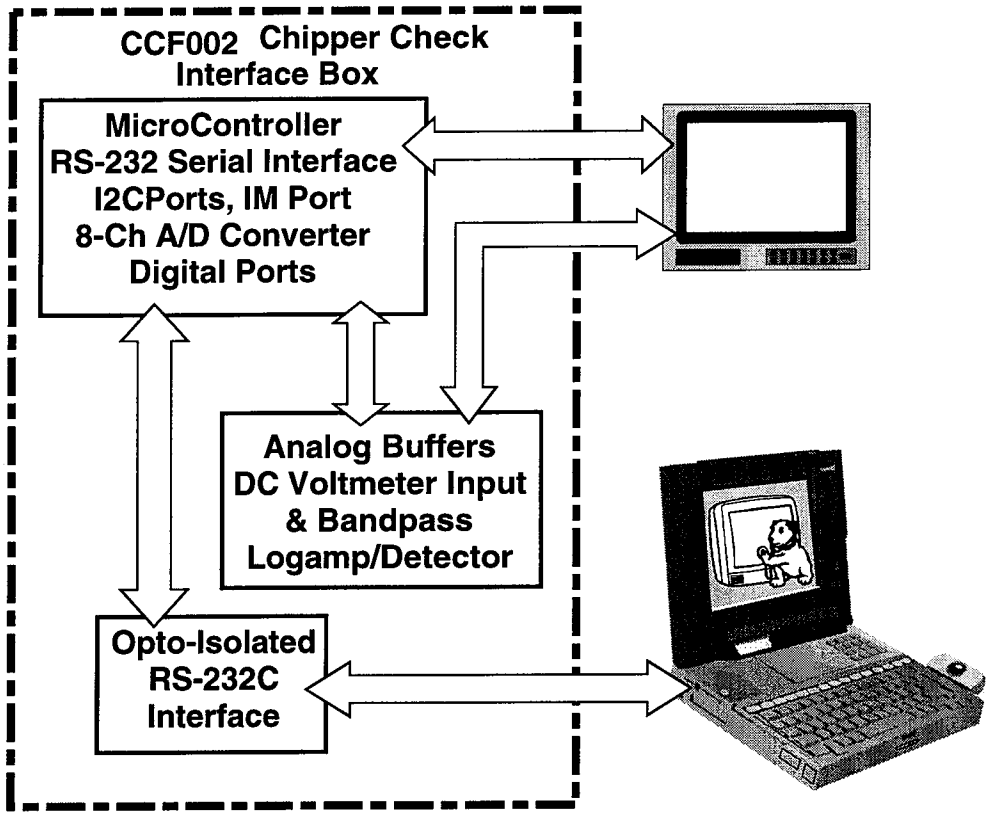
Figure 12-2, CTC203 Video Signal Path



Chipper Check™

Chipper Check™ Overview

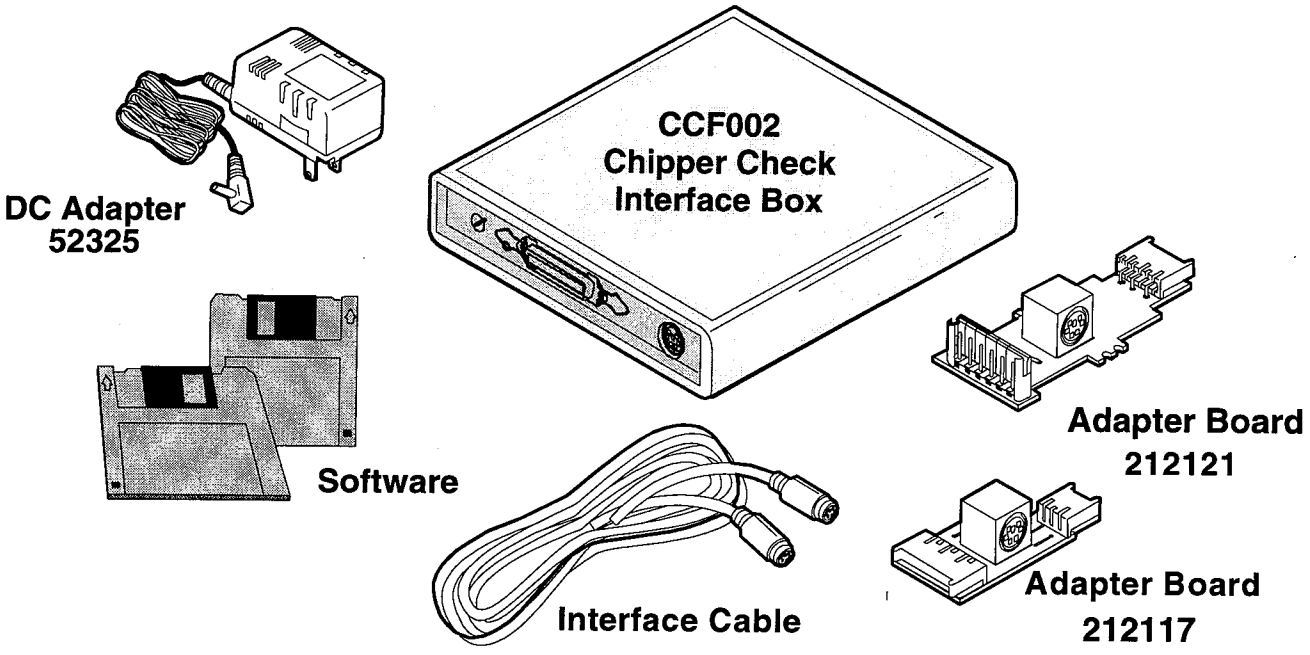
The evolution from early analog televisions to the modern digitally controlled TV has produced a number of new challenges for the service technician. These new microcomputer controlled televisions can exhibit a variety of symptoms that do not follow the logic of older analog television receivers. In addition, the alignments are no longer performed by adjusting a potentiometer, rather they have been replaced by a digital value that is stored in memory and converted to a DC voltage that is applied to the appropriate circuit. At first, this type of system can be confusing since it is not always obvious which adjustment is being performed by simply looking at the display on the picture tube. Some adjustments are not incorporated until the receiver is turned off and back on, which makes it very difficult to know when the adjustment is correct. Chipper Check™ was developed to address these differences and to provide the technician with a convenient method of performing adjustments and diagnosing problems. The Chipper Check™ system is composed of two (2) major components. The first component and the most visible is the hardware interface. The interface is responsible for physically connecting the TV and personal computer together. The second part is the software that runs the personal computer. This software provides the instructions on what to do and how to do it.



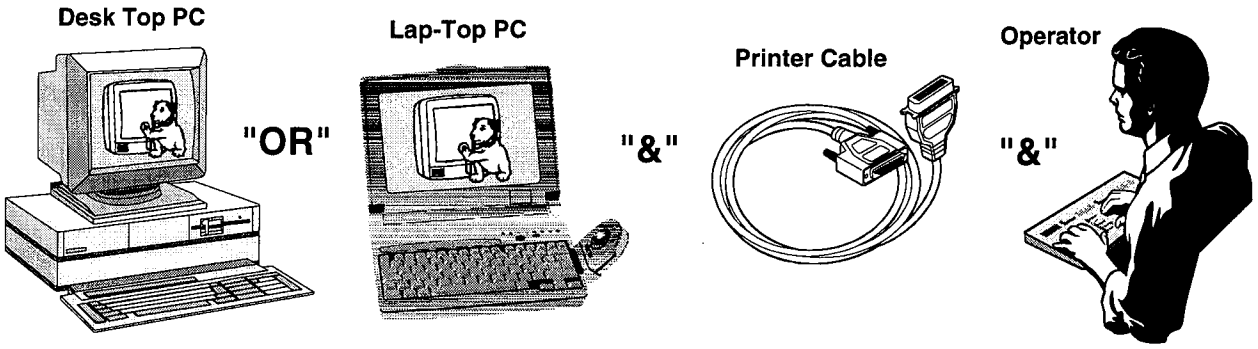
Chipper Check Simplified Block Diagram

Chipper Check™ Hardware

The hardware consists of small adapter boards that attach directly to the chassis via a communications port, an interconnect cable and the Chipper Check™ interface box. A standard parallel printer cable is used to connect the interface box to the parallel port on the personal computer, however this cable is not part of the Chipper Hardware package. The adapter board allows the flexibility of connecting the interface box to a number of different chassis families. The communications format may vary from one chassis family to the next, and rather than developing a new interface box for each chassis, changing the adapter board allows the same interface box to be used. The Chipper Check™ interface box provides electrical isolation between the personal computer and the television receiver under test. The portion of the interface which connects to the personal computer is powered from the computer's parallel port. The interface contains a power supply that provides power to the television receiver side of the interface. The interface converts the signals from the parallel port of the computer into the correct protocol for the television microprocessor.

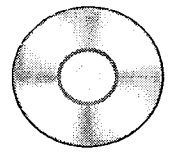


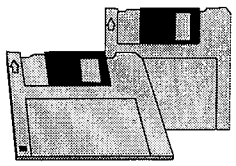
Chipper Check Items



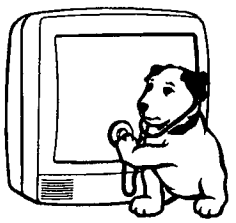
Chipper Check Items "Not Supplied"

Chipper Check™ Software





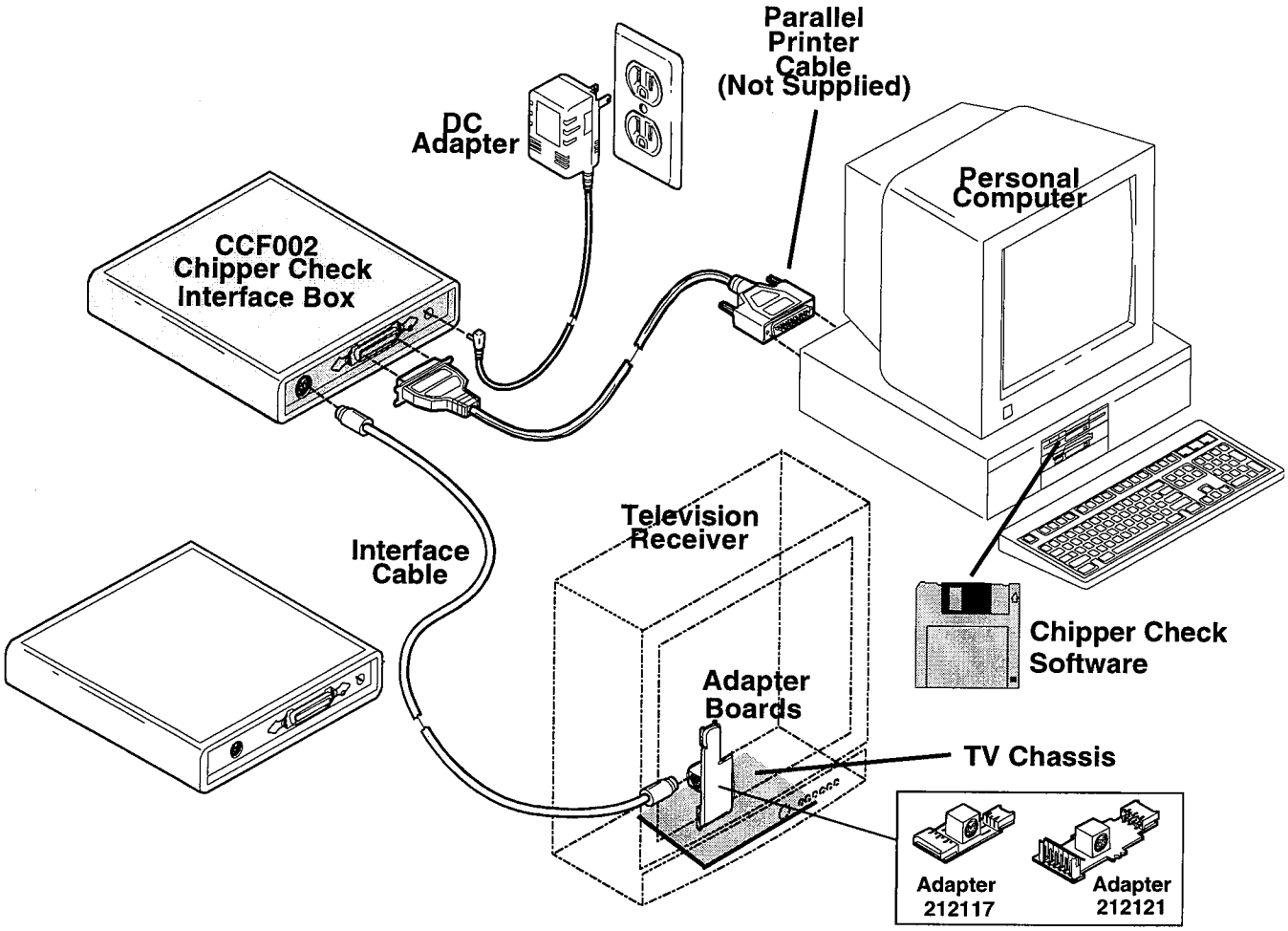
The Chipper Check™ software allows the technicians PC (personal computer) to troubleshoot, communicate with and perform alignments in a digitally controlled television. The Chipper Check™ software is composed of many different routines that are unique to each major chassis family. There is also a set of standard drivers for the interface hardware that are used for all chassis families. The software has been designed to be easily updated as new chassis and models are introduced. The software contains chassis auto-detection function, customer information screens, diagnostic routines, alignment routines along with on-line help files to guide the technician. The chassis auto-detection is used to ensure that only the alignments required for a specific chassis are performed. The customer information screen allows the service technician a way to match the information stored by Chipper Check™ to the specific instrument being serviced. The diagnostic routines are used to read any error codes stored in the instrument and identify which integrated circuit in the chassis is not responding. The alignment routines provides all alignment procedures needed on each chassis. The help files provide information on how to use the software how to perform the alignments, test point locations, and troubleshooting tips.



Chipper Check™

"Dead Set" Troubleshooting with Chipper Check™

Chipper Check™ has two basic modes of operation, **"Dead Set"** and **"Normal"**. The dead set mode is helpful when the television receiver does not turn on. Chipper Check™ can be used to read the fault codes that were stored in the EEPROM. These fault codes remain in the EEPROM as long as there is standby power to the EEPROM. In this mode, the chassis auto-detection feature does not function, so the chassis type must be manually selected from a list. When the fault codes are recovered they indicate to the technician which IC was not responding to the microprocessor. It is important to remember that this does not necessarily mean the IC called out is defective, merely that it is not communicating with the microprocessor. The reason for this could well be



something other than the IC itself, such as a external component on the IC, etc. However, it does give the technician a good starting point for troubleshooting a "Dead Set". Likewise, if the standby power supply is not functioning, Chipper Check™ cannot read the error codes. This situation indicates the problem is probably located in the standby power supply and the technician should not require Chipper Check™ to find power supply failures. In addition to reading the fault codes, it is possible to read and store the contents of the EEPROM's. The contents of the EEPROM's are stored in a customer file which allows the original settings to be reinstalled in the EEPROM after troubleshooting the dead set. The PIP EEPROM data cannot be read or re-initialized in the dead set mode.

Chipper Check™ Hookup

To use Chipper Check™ in the normal mode, it is necessary to place the television microprocessor in the "slave" mode to prevent communication problems with the interface hardware. The adapter board and cable is connected to the Chipper Check™ port on the television chassis before the television is turned on, as long as the other end of the cable is not connected to the interface box. Having both ends of the cable connected may load the communications lines and prevent the television from turning on. After the television is in the slave mode and the cable is connected to the interface box, the Chipper Check™ software can be started.

Chipper Check™ Operation

The first thing the program does is to check communications between the television and the computer. Part of this process is to detect which chassis is connected. If the wrong chassis is detected, it is possible to select the correct chassis type. Use caution when changing chassis types because the alignments are different, and selecting the wrong chassis can cause the computer to lock up, or store incorrect information in the television EEPROM. After communications are established, a customer information screen appears. This allows customer information such as name and model/serial number data to be stored. It is important to note that when the information on this screen is saved, the contents of the EEPROM are not yet associated with the file. This screen is placed here as a convenience to the service technician. The customer information or job ticket number, etc. is stored at the beginning of the process when the information is still readily available.

Diagnostic Function

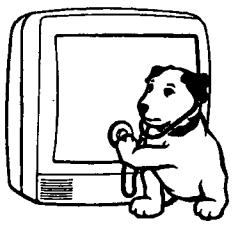
The next screen after the customer information gives three choices, diagnostics, alignments, or a major part that has been replaced. The diagnostic portion gives the option of reading fault codes, checking the EEPROM, or reinitializing the EEPROM. The fault code again tells you which major component or IC is not responding. However, it does not tell you why that component is not responding. This simply indicates an area of problems. When the EEPROM is checked, data is ***"written to"*** and ***"read from"*** every location in the EEPROM. If the computer can read and write to every location, the EEPROM is functioning correctly and should not be replaced. However, this does not mean that the data stored in the EEPROM is correct. For this reason, the option of re-initializing the EEPROM is provided. Initializing the EEPROM will write the ***"factory values"*** to certain locations of the EEPROM. These are the items that need to be set to certain values to ensure proper initial operation. None of the alignment data is modified, nor is customer information such as scan lists and channel labels changed. During initialization, the customer controls are set to the factory preset values. These include the convergence settings on projection sets.

Alignments Function

The alignment function has the service alignments grouped into circuit areas or by the effect they have on the picture. Each group of alignments are performed in the proper order for that group. That is, once a group of alignments is selected, they should be performed in the order indicated, but the order in which the groups are selected does not matter. The highlighted text in the alignment procedure shows test point locations on the chassis and gives other helpful tips on performing the alignment. The help button on the alignment screen provides information on what to do if the alignment cannot be adjusted properly.

Part Replaced Function

The last option is ***"Replaced Part".*** When this option is selected, the technician must enter which major part has been replaced. The Chipper Check™ software then steps the technician through all alignments that should be performed or checked after that part has been changed. For example, if a component was changed in the PIP tuner, all PIP tuner alignments should be checked, however it is not necessary to perform the PIP color and tint alignments so these would not be brought up.



Chipper Check™

Error Codes

There are three EEPROM locations specifically holding error codes noted by the software routine of the chassis. On the front panel menu, they are located in positions 1, 2 and 3 after entering the security address and contain a digital readout of the code. Chipper Check™ also reads these three locations and places a text translation to each code.

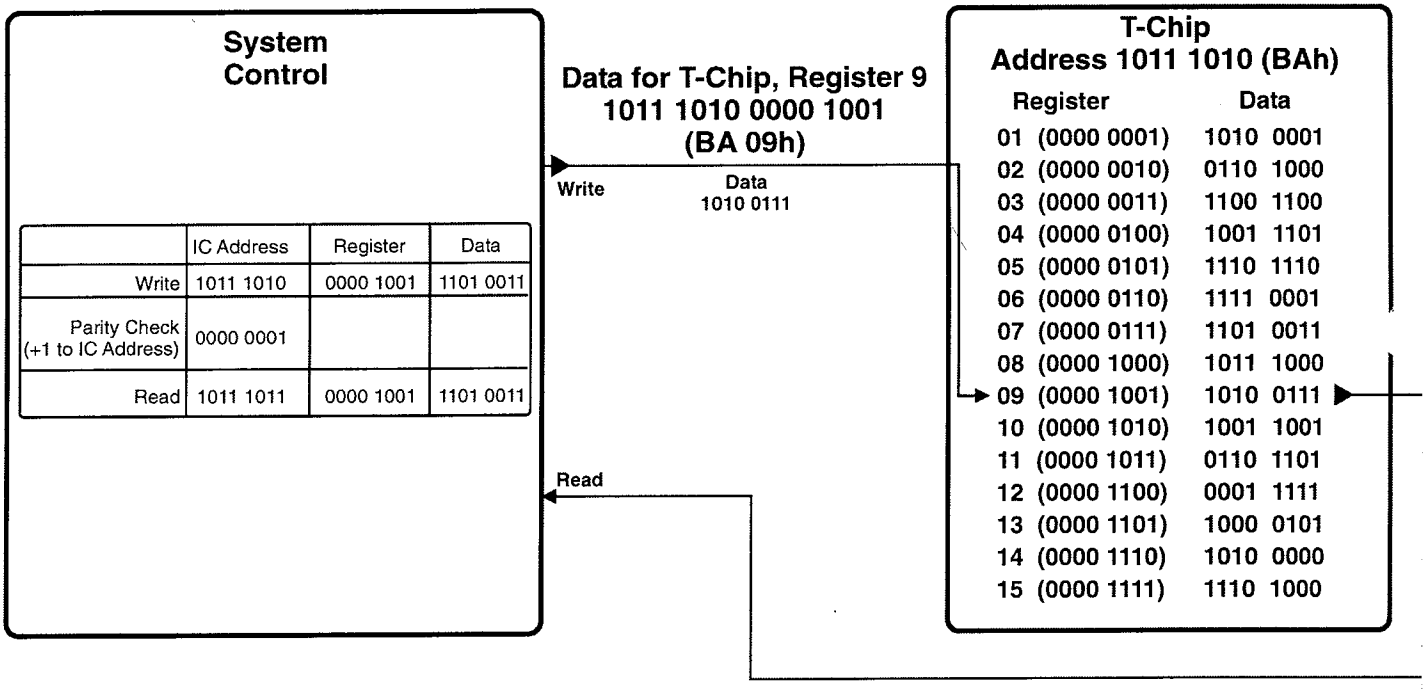
Error Code Location	Possible Error Code	Text Explanation
1	7	Scan Loss
2	3	+12V Run Supply
3	192	2nd Tuner PLL

In all cases, error location #1 is the first code logged by the system control microprocessor since the last time all three error code locations were cleared. Location #2 is the second code logged since the locations were cleared. Location #3 is the most important location as it contains the most recent code logged by system control. In theory, there may have been hundreds of codes logged between #2 and #3. It would be good practice to write down the codes in each location and reset all three locations to zero. Then, upon attempting a restart of the set, a current error code list will be generated that may prove more useful to the technician in trouble-shooting efforts.

In the above example, locations 1 and 2 could have occured at any time from the original manufacture of the set to the most recent startup attempt. Generally, without knowing when the first two errors were logged, only error code 3, a 2nd tuner PLL IC failure, may be considered current and useful. After successfull completion of any repair efforts, all three error code locations should be set to zero.

A second important point of the error code list is how they are generated and how they are checked. When Chipper Check™ or System Control sends information to an IIC device it is in the form of complete words. Most IIC devices acknowledge the receipt of data by sending the same data back to the micro via the sending address "plus one". This is known as a "parity" check.

For example, in the CTC179 chassis, EEPROM data sent to the T2, register 09 in binary would look like this: 1011 1010 0000 1001. The first byte contains the T2 address, 1011 1010 (BAh). The next is the address of the register inside the T2, 0000 1001 (09h). This would be followed by the actual data byte, in our example 1010 0111. When the T-Chip acknowledges it has received new data for the register, it changes the address BA, incrementing it by one to become BB. The T-Chip register address and data remain the same. System Control compares the outgoing data with the returning data for these two addresses. If the two match, normal operation is continued. If they do not, an error code is logged.



	IC Address	Register	Data
Write	1011 1010	0000 1001	1101 0011
Parity Check (+1 to IC Address)	0000 0001		
Read	1011 1011	0000 1001	1101 0011

The chassis may or may not go into the "batten" routine depending upon which error is logged. This may also cause "unidentified" errors to be generated in the service menu. Depending upon software the error code could be logged as either the outgoing address or the parity address. In this case, the T-Chip address is BA, which is logged in the error codes in decimal notation or 186. The returning address is BB, or decimal 187. Either code may show up in the error codes, but they should be taken to mean a communication error with the T-Chip.

The error codes do not necessarily mean a specific IC failure. They simply indicate data was sent to a specific address and not written into the register correctly, according to the parity check routine. This could mean something as simple as a temporary read/write error, as severe as a catastrophic device failure or something in between. Keep in mind many other factors can cause a read/write error. The error codes are simply meant to aid in failure diagnosis by steering the technician in the proper direction. They cannot troubleshoot a chassis. Begin by checking power supplies to the device. Then check IIC clock and data lines. Finally check all signal lines. The technician must still "prove" device failure. Chipper Check™ nor the error codes are capable of identifying specific hardware failure.

Initialization & Customer Files

When checking an EEPROM for possible failure or corrupt data, the technician has two options before performing the EEPROM Test. Chipper Check™ allows the technician to either "Initialize" the EEPROM or store/retrieve a "Customer" file. There are important differences in the two files.

First, there are several locations for data in the EEPROM which are not used in field service. This is data set at the time of manufacturer and does not require adjustment, alignment or checking by the technician. However, as with any EEPROM, the data in those locations may become corrupt for any number of reasons yet the EEPROM will otherwise be fully functional. The initialization file, different for each chassis version, resets *only these initialization locations* to factory default settings for the specific chassis. No other data is touched by the file.

A customer file saves the data in *every location* of the EEPROM to the PC's drive for future recovery. This includes data in the locations that are also in the initialization file. Unfortunately, Chipper Check can not determine whether the data is corrupt. The customer file is useful if an EEPROM must be replaced or for use in troubleshooting faulty EEPROM data. It should be saved to a unique file name. If an EEPROM is replaced, the customer file may then be loaded back into the EEPROM. All alignments, customer settings and the initialization string are recovered. Since the EEPROM was replaced, some data contained in it may be corrupt. The technician should check the set very carefully prior to returning it to service. The proper order to restore the EEPROM is; customer file first, then re-initialize!

Chipper Check™ DOES NOT check the values in the EEPROM for validity, it only checks to see if all EEPROM address locations can be read and written to.

Further Reading

Remember, Chipper Check™ is not a troubleshooter used to replace technical knowledge. It is meant as another tool, much like a scope or DVM the technician may use for troubleshooting and performing alignments on TCE television chassis'.

Thomson Consumer Electronics Technical Publications has released a Chipper Check™ User Guide. In it are instructions on installing the software, hints for navigating around the interface, connecting to the chassis, modes, shortcuts, all about error codes and many other useful details. Order TCE Publication #T-CCUM.

The following charts show the CATV band channel assignments and frequencies. The CTC203 requires alignment of a select number of these channels (shown in highlight). Proper alignment of the CATV alignment channels provides system control with the information to calculate or *interpolate* the remaining channels properly. The CATV band is broken into 3 smaller bands for purposes of alignment and channel selection. These bands do not correspond to the FCC channel allocation bands, but are simply frequency bands selected to provide ease of tuning within the CTC203.

Cable Channel		Pix Freq.	Sound Freq.	LO Freq.
Band1	2	55.25	59.75	101.00
	3	61.25	65.75	107.00
	4	67.25	71.75	113.00
	1	73.25	77.75	119.00
	5	77.25	81.75	123.00
	6	83.25	87.75	129.00
	6 IRC	85.25	89.75	131.00
	95	91.25	95.75	137.00
	96	97.25	101.75	143.00
	97	103.25	107.75	149.00
	98	109.25	113.75	155.00
	99	115.25	119.75	161.00
	14	121.25	125.75	167.00
	15	127.25	131.75	173.00
	16	133.25	137.75	179.00
	17	139.25	143.75	185.00

Cable Channel		Pix Freq.	Sound Freq.	LO Freq.
Band 2	18	145.25	149.75	191.00
	19	151.25	155.75	197.00
	20	157.25	161.75	203.00
	21	163.25	167.75	209.00
	22	169.25	173.75	215.00
	7	175.25	179.75	221.00
	8	181.25	185.75	227.00
	9	187.25	191.75	233.00
	10	193.25	197.75	239.00
	11	199.25	203.75	245.00
	12	205.25	209.75	251.00
	13	211.25	215.75	257.00
	23	217.25	221.75	263.00
	24	223.25	227.75	269.00
	25	229.25	233.75	275.00
	26	235.25	239.75	281.00
	27	241.25	245.75	287.00
	28	247.25	251.75	293.00
	29	253.25	257.75	299.00
	30	259.25	263.75	305.00
	31	265.25	269.75	311.00
	32	271.25	275.75	317.00
	33	277.25	281.75	323.00
	34	283.25	287.75	329.00
	35	289.25	293.75	335.00
	36	295.25	299.75	341.00
	37	301.25	305.75	347.00
	38	307.25	311.75	353.00
	39	313.25	317.75	359.00
	40	319.25	323.75	365.00
	41	325.25	329.75	371.00
	42	331.25	335.75	377.00
	43	337.25	341.75	383.00
	44	343.25	347.75	389.00
	45	349.25	353.75	395.00
	46	355.25	359.75	401.00
	47	361.25	365.75	407.00
	48	367.25	371.75	413.00
	49	373.25	377.75	419.00
	50	379.25	383.75	425.00

Cable Channel		Pix Freq.	Sound Freq.	LO Freq.
Band 3	51	385.25	389.75	431.00
	52	391.25	395.75	437.00
	53	397.25	401.75	443.00
	54	403.25	407.75	449.00
	55	409.25	413.75	455.00
	56	415.25	419.75	461.00
	57	421.25	425.75	467.00
	58	427.25	431.75	473.00
	59	433.25	437.75	479.00
	60	439.25	443.75	485.00
	61	445.25	449.75	491.00
	62	451.25	455.75	497.00
	63	457.25	461.75	503.00
	64	463.25	467.75	509.00
	65	469.25	473.75	515.00
	66	475.25	479 75	521.00
	67	481.25	485.75	527.00
	68	487.25	491 75	533.00
	69	493.25	497.75	539.00
	70	499.25	503.75	545.00
	71	505.25	509.75	551.00
	72	511.25	515.75	557.00
	73	517.25	521.75	563.00
	74	523.25	527.75	569.00
	75	529.25	533.75	575.00
	76	535.25	539 75	581.00
	77	541.25	545 75	587.00
	78	547.25	551.75	593.00
	79	553.25	557.75	599.00
	80	559.25	563.75	605.00
	81	565.25	569.75	611.00
	82	571.25	575 75	617.00
	83	577.25	581.75	623.00
	84	583.25	587.75	629.00
	85	589.25	593.75	635.00
	86	595.25	599.75	641.00
	87	601.25	605.75	647.00
	88	607.25	611.75	653.00

Cable Channel		Pix Freq.	Sound Freq.	LO Freq.
Band 3	89	613.25	617.75	659
	90	619.25	623.75	665
	91	625.25	629.75	671
	92	631.25	635.75	677
	93	637.25	641.75	683
	94	643.25	647.75	689
	95	91.25	95.75	137
	96	97.25	101.75	143
	97	103.25	107.75	149
	98	109.25	113.75	155
	99	115.25	119.75	161
	100	649.25	653.75	695
	101	655.25	659.75	701
	102	661.25	665.75	707
	103	667.25	671.75	713
	104	673.25	677.75	719
	105	679.25	683.75	725
	106	685.25	689.75	731
	107	691.25	695.75	737
	108	697.25	701.75	743
	109	703.25	707.75	749
	110	709.25	713.75	755
	111	715.25	719.75	761
	112	721.25	725.75	767
	113	727.25	731.75	773
	114	733.25	737.75	779
	115	739.25	743.75	785
	116	745.25	749.75	791
	117	751.25	755.75	797
	118	757.25	761.75	803
	119	763.25	767.75	809
	120	769.25	773.75	815
	121	775.25	779.75	821
	122	781.25	785.75	827
	123	787.25	791.75	833
	124	793.25	797.75	839
	125	799.25	803.75	845

The following charts show the off-air or *broadcast* band channel assignments and frequencies. The CTC203 does not require any alignment of these channels. Proper alignment of the CATV channels provides system control with the information to select the channels properly. The broadcast band is broken into 2 smaller bands for purposes of alignment and channel selection.

OFF-AIR CHANNEL		PIX FREQ.	SOUND FREQ.	LO FREQ.
Band 1	2	55.25	59.75	101.00
	3	61.25	65.75	107.00
	4	67.25	71.75	113.00
	5	77.25	81.75	123.00
	6	83.25	87.75	129.00
	7	175.25	179.75	221.00
	8	181.25	185.75	227.00
	9	187.25	191.75	233.00
	10	193.25	197.75	239.00
	11	199.25	203.75	245.00
	12	205.25	209.75	251.00
	13	211.25	215.75	257.00

OFF-AIR CHANNEL		PIX FREQ.	SOUND FREQ.	LO FREQ.
Band 3	14	471.25	475.75	517.00
	15	477.25	481.75	523.00
	16	483.25	487.75	529.00
	17	489.25	493.75	535 00
	18	495.25	499.75	541.00
	19	501.25	505.75	547 00
	20	507.25	511.75	553.00
	21	513.25	517.75	559.00
	22	519.25	523.75	565.00
	23	525.25	529.75	571.00
	24	531.25	535.75	577.00
	25	537.25	541.75	583.00
	26	543.25	547.75	589.00
	27	549.25	553.75	595.00
	28	555.25	559.75	601.00
	29	561.25	565.75	607.00
	30	567.25	571.75	613.00
	31	573.25	577.75	619.00
	32	579.25	583.75	625.00
	33	585.25	589.75	631.00
	34	591.25	595.75	637.00
	35	597.25	601.75	643.00
	36	603.25	607.75	649.00
	37	609.25	613.75	655.00
	38	615.25	619.75	661.00
	39	621.25	625.75	667.00
	40	627.25	631.75	673.00
	41	633.25	637.75	679.00

OFF-AIR CHANNEL		PIX FREQ.	SOUND FREQ.	LO FREQ.
Band 3	42	639.25	643.75	685.00
	43	645.25	649.75	691.00
	44	651.25	655.75	697
	45	657.25	661.75	703
	46	663.25	667.75	709
	47	669.25	673.75	715
	48	675.25	679.75	721
	49	681.25	685.75	727
	50	687.25	691.75	733
	51	693.25	697.75	739
	52	699.25	703.75	745
	53	705.25	709.75	751
	54	711.25	715.75	757
	55	717.25	721.75	763
	56	723.25	727.75	769
	57	729.25	733.75	775
	58	735.25	739.75	781
	59	741.25	745.75	787
	60	747.25	751.75	793
	61	753.25	757.75	799
	62	759.25	763.75	805
	63	765.25	769.75	811
	64	771.25	775.75	817
	65	777.25	781.75	823
	66	783.25	787.75	829
	67	789.25	793.75	835
	68	795.25	799.75	841
	69	801.25	805.75	847